

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- 35-ns access time
- Low active power
 - 440 mW
- Low standby power (7C148)
 - 55 mW (all others)
- 5-volt power supply ± 10% tolerance, both commercial and military
- TTL-compatible inputs and outputs

Functional Description

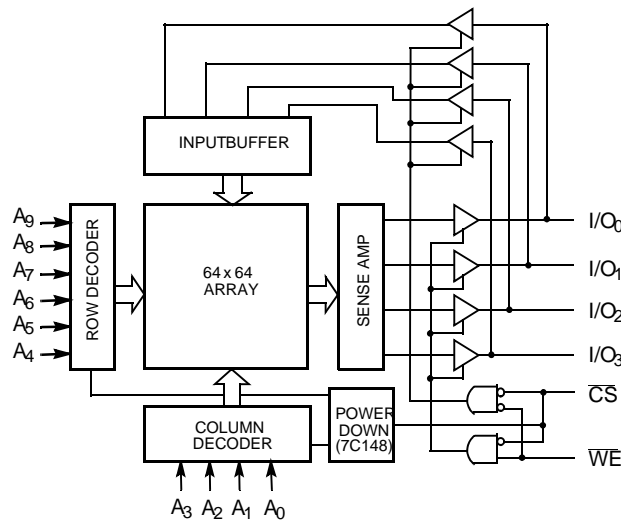
The CY7C148 is a high-performance CMOS static RAMs organized as 1024 by 4 bits. Easy memory expansion is provided by an active LOW chip select (\overline{CS}) input and three-state outputs. The CY7C148 remains in a low-power mode as long as the device remains unselected; i.e., (\overline{CS}) is HIGH, thus reducing the average power requirements of the device.

Writing to the device is accomplished when the chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the I/O pins (I/O_0 through I/O_3) is written into the memory locations specified on the address pins (A_0 through A_9).

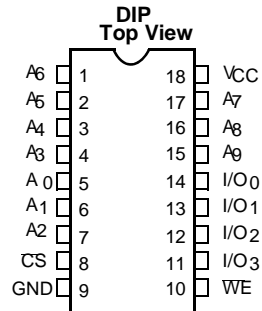
Reading the device is accomplished by taking chip select (\overline{CS}) LOW while write enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data I/O pins.

The I/O pins remain in a high-impedance state when chip select (\overline{CS}) is HIGH or write enable (\overline{WE}) is LOW.

Logic Block Diagram



Pin Configuration



Selection Guide

Description		7C148-35
Maximum Access Time (ns)		35
Maximum Operating Current (mA)	Commercial	80
Maximum Standby Current (mA)	Commercial	10

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9).....	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V

DC Input Voltage	-3.0V to +7.0V
Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current.....	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[1]

Parameter	Description	Test Conditions	7C148-35		Unit	
			Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V	
V _{IH}	Input HIGH Voltage		2.0	6.0	V	
V _{IL}	Input LOW Voltage		-3.0	0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-10	10	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-50	50	μA	
I _{CC}	V _{CC} Operating Supply Current	Max. V _{CC} , CS ≤ V _{IL} , Output Open	Com'l	80	mA	
I _{SB}	Automatic CS Power-Down Current	Max. V _{CC} , CS ≥ V _{IH}	7C148 Only	Com'l	10	mA
I _{PO}	Peak Power-On Current ^[1]	Max. V _{CC} , CS ≥ V _{IH}	7C148 Only	Com'l	10	mA

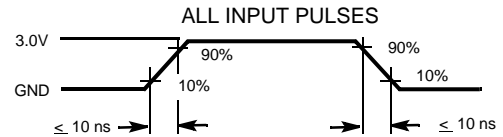
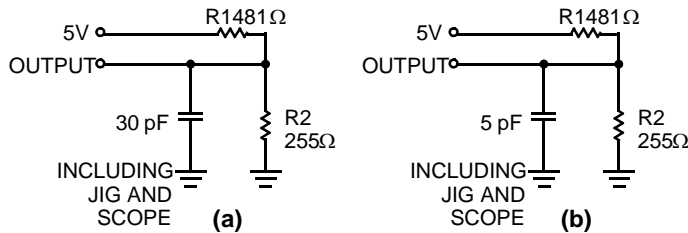
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	8	pF
C _{OUT}	Output Capacitance		8	pF

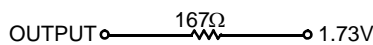
Notes

1. A pull-up resistor to V_{CC} on the $\overline{\text{CS}}$ input is required to keep the device deselected during V_{CC} power-up. Otherwise current will exceed values given (CY7C148 only).
2. For test purposes, not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[1]

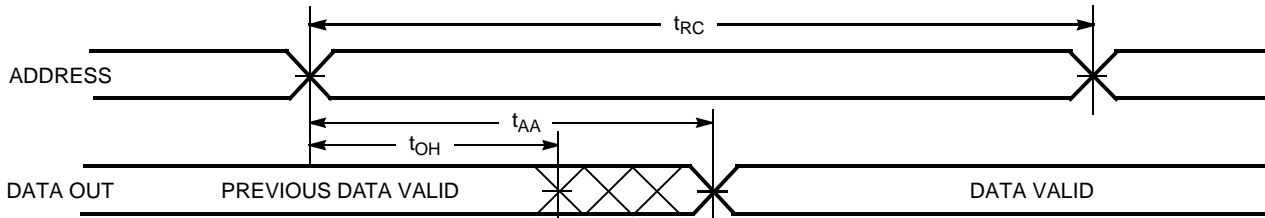
Parameter	Description	7C148-35		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)	35		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)		35	ns
t_{ACS1}	Chip Select LOW to Data Out Valid		35	ns
t_{ACS2}			35	ns
$t_{LZ}^{[6]}$	Chip Select LOW to Data Out On	10		ns
$t_{HZ}^{[6]}$	Chip Select HIGH to Data Out Off	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time	0		ns
t_{PD}	Chip Select HIGH to Power-Down Delay		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	0		ns
WRITE CYCLE				
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)	35		ns
$t_{WP}^{[7]}$	Write Enable LOW to Write Enable HIGH	30		ns
t_{WR}	Address Hold from Write End	5		ns
$t_{WZ}^{[6]}$	Write Enable to Output in High Z	0	8	ns
t_{DW}	Data in Valid to Write Enable HIGH	20		ns
t_{DH}	Data Hold Time	0		ns
t_{AS}	Address Valid to Write Enable LOW	0		ns
$t_{CW}^{[7]}$	Chip Select LOW to Write Enable HIGH	30		ns
$t_{OW}^{[6]}$	Write Enable HIGH to Output in Low Z	0		ns
t_{AW}	Address Valid to End of Write	30		ns

Notes:

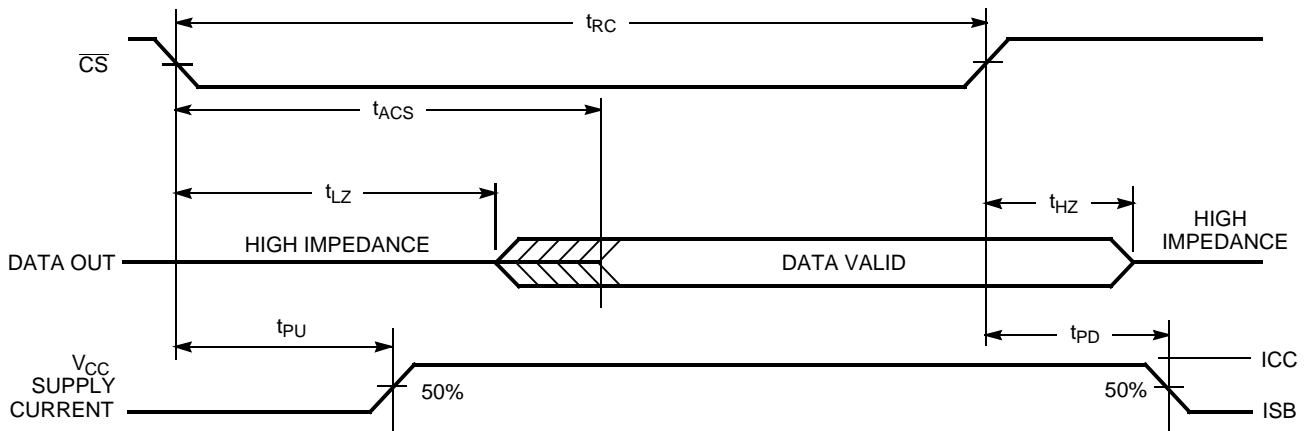
- Chip deselected greater than 25 ns prior to selection.
- Chip deselected less than 25 ns prior to selection.
- At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ± 500 mV from steady-state voltage with specified loading in part (b) of AC Test Loads.
- The internal write time of the memory is defined by the overlap of \overline{CS} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

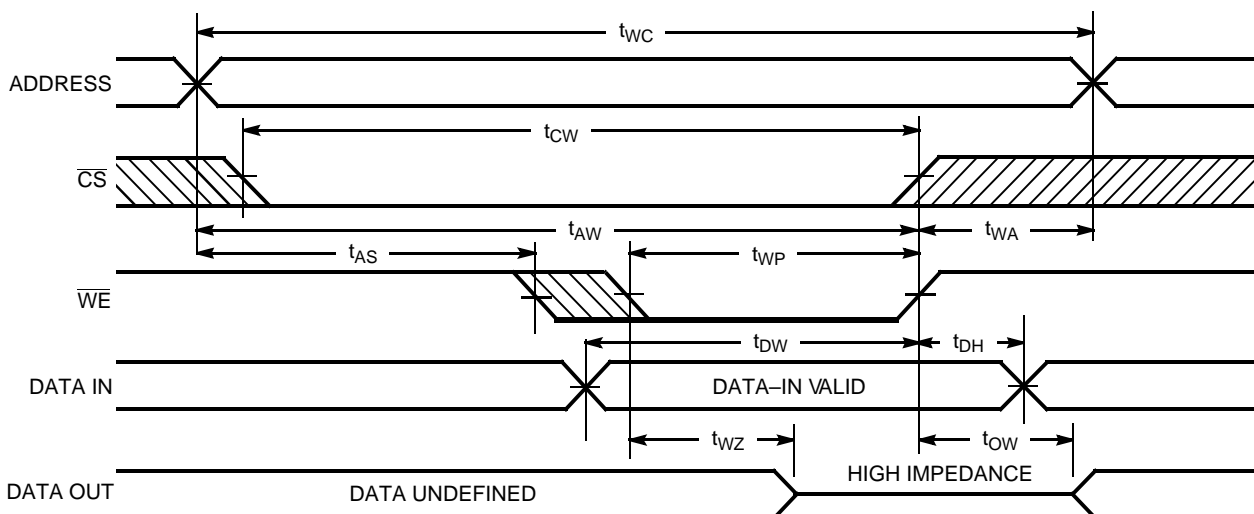
Read Cycle No.1 [8,9]



Read Cycle No.2 [8,10]



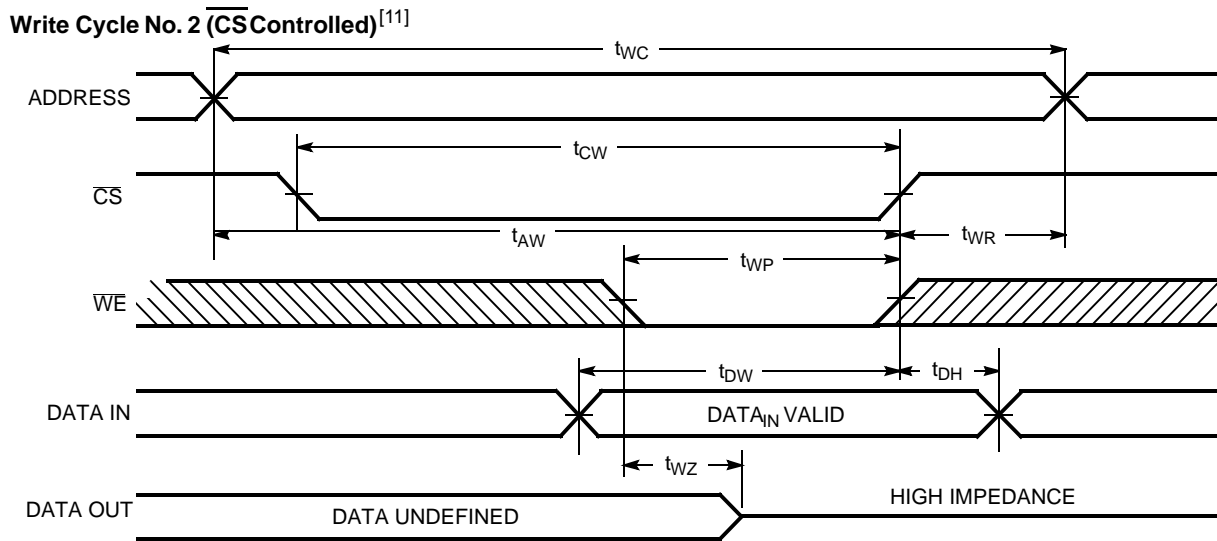
Write Cycle No.1 (\overline{WE} Controlled)



Notes

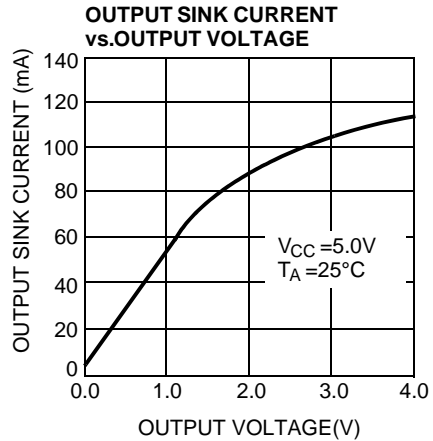
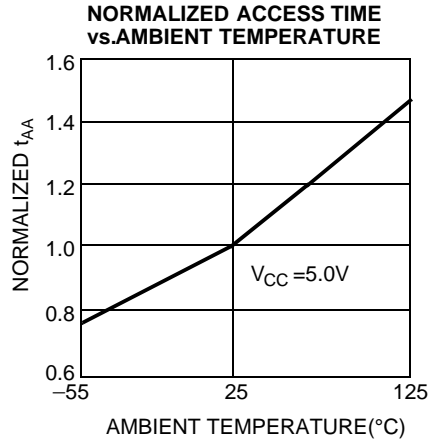
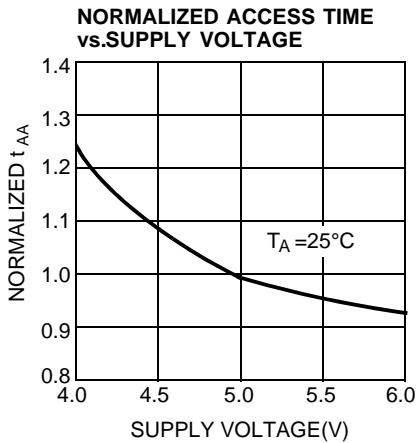
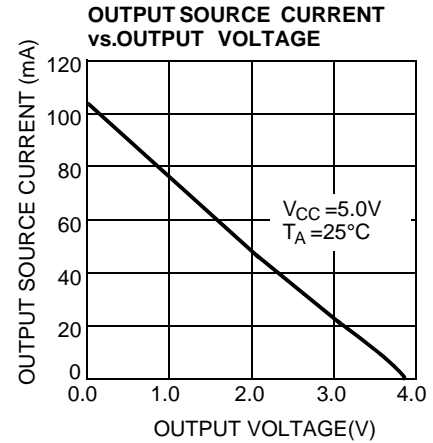
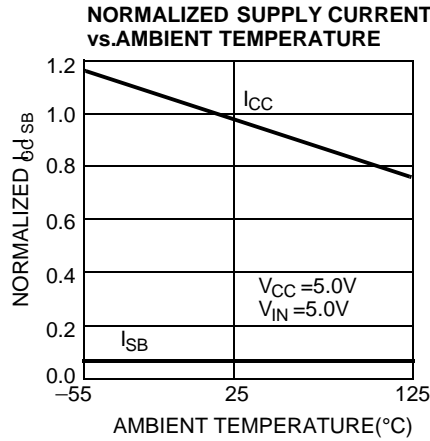
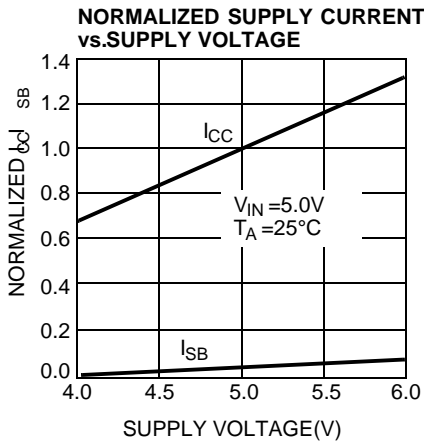
8. \overline{WE} is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with \overline{CS} transition LOW.

Switching Waveforms (continued)

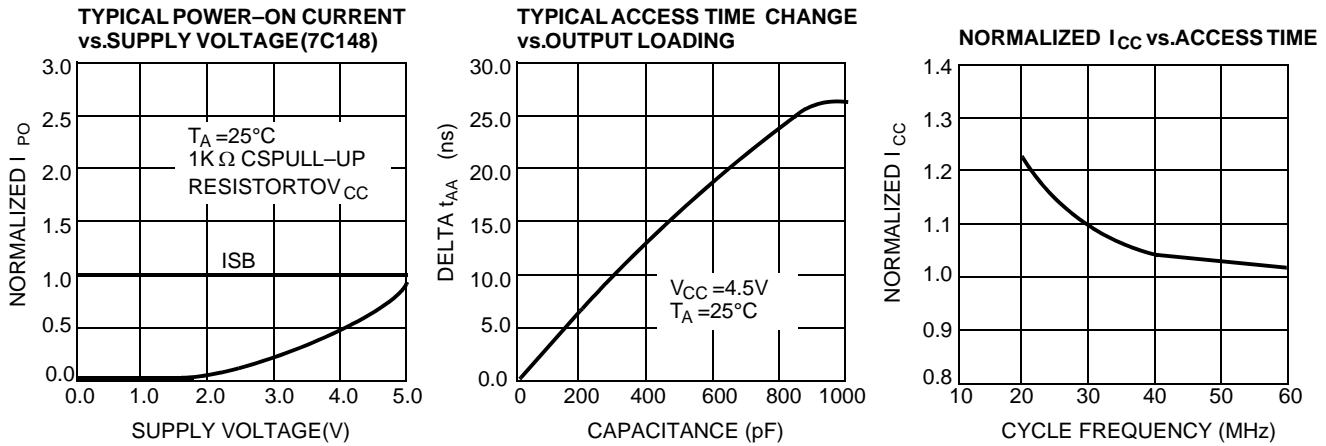


Note:
 11. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



Typical DC and AC Characteristics

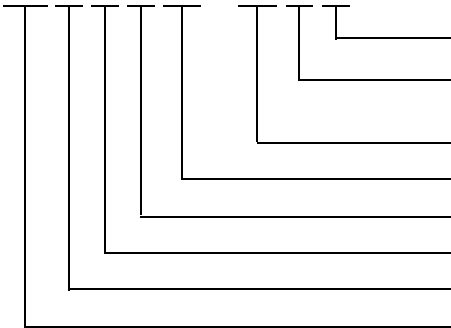


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
35	CY7C148-35PC	P3	18-Lead (300-Mil) Molded DIP	Commercial

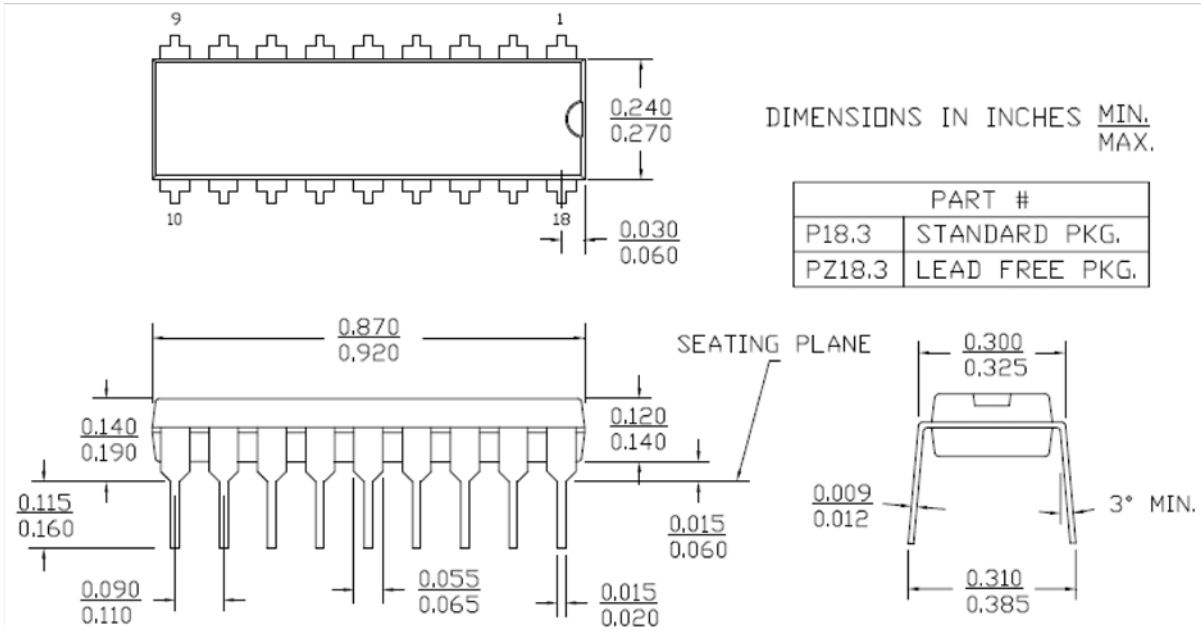
Ordering Code Definitions

CY 7 C 1 48 - 35 P C



Temperature Range: C = Commercial
 Package Type:
 P: 18-Lead Molded DIP
 Access time in ns
 48 = 4-Kbit density with Data width \times 4 bits
 1 = Fast Asynchronous SRAM family
 Technology Code: C = CMOS
 7 = SRAM
 CY = Cypress

Figure 1. 18-Lead (300-Mil) Molded DIP P3



51-85010 *C

Document History Page

Document Title: CY7C148 1K x 4 Static RAM Document Number: 38-05059				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	110170	09/29/01	SZV	Change from Spec number: 38-00031 to 38-05059
*A	2894016	03/19/2010	VKN	Removed 25 ns speed bin Removed Military product information Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Removed 18-pin (300-mil) CerDIP and 18-pin Rectangular Leadless Chip Carrier packages Updated ordering Information Table
*B	3051744	10/07/2010	PRAS	Removed inactive part CY7C149-45PC from all places it appeared. Added Ordering Code Definition Updated Package Diagram

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