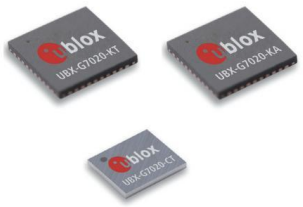
UBX-G7020

u-blox 7 GPS/GNSS chips

Hardware Integration Manual

Highlights:

- u-blox 7 position engine featuring excellent accuracy and time-to-first-fix performance
- Multi-GNSS engine for GPS, GLONASS, Galileo and QZSS
- AssistNow Online, Offline and Autonomous for faster TTFF
- Minimal board space
- Low power consumption
- Minimal e-BOM



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Document Information	
Title	UBX-G7020
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Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	ROM/FLASH version	PCN reference
UBX-G7020-KT QFN40 package (Standard grade)	UBX-G7020-KT-A0100 A	1.00	N/A
UBX-G7020-CT WL-CSP50 (Standard grade)	UBX-G7020-CT-A0100 A	1.00	N/A
UBX-G7020-KA QFN40 package (Automotive grade)	UBX-G7020-KA-A0100 A	1.00	N/A

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Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **GPS Compendium:** This document, also known as the GPS book, provides a wealth of information regarding generic questions about GPS system functionalities and technology.
- **Receiver Description and Protocol Specification:** Messages, configuration and functionalities of the u-blox 7 software releases and receivers are explained in this document.
- **Hardware Integration Manual:** This Manual provides hardware design instructions and information on how to set up production and final product tests.
- **Application Note:** This document provides general design instructions and information that applies to all u-blox GPS receivers. See section Related documents for a list of Application Notes related to your GPS receiver.

How to use this manual

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to chipset integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the receiver.**

Questions

If you have any questions about u-blox 7 Hardware Integration, please:

- Read this manual carefully.
- Contact our information service on the homepage www.u-blox.com.
- Read the questions and answers on our FAQ database on the homepage.

Technical support

Worldwide web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

If you have technical problems or cannot find the required information in the provided documents, contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful information when contacting technical support

When contacting Technical Support please have the following information ready:

- Chipset type (e.g. UBX-G7020-KT) and revision (e.g. A0100)
- Receiver configuration
- Schematic at least of the GPS section of your circuit
- Layout of the GPS section of your circuit and the PCB stack-up.
- Clear description of your question or the problem together with a u-center logfile
- A short description of the application
- Your complete contact details

Contents

1 Hardware Description

1.1 Overview

Featuring a single die solution, low power consumption and low costs, the UBX-G7020 GPS/GNSS chips are multi-GNSS (GPS, GLONASS, Galileo, QZSS and SBAS) positioning chips developed to meet the requirements of an extensive range of applications and end-products. Based on the high performance u-blox 7 position engine, these receivers provide exceptional sensitivity and acquisition times without requiring an external host. u-blox' advanced RF-design and interference suppression measures enable reliable positioning even in difficult signal conditions.

u-blox 7 technology delivers high performance with low power consumption and low costs. An integrated DC/DC converter and intelligent power management are breakthroughs for low-power applications. The minimal BOM requires as few as 8 external components and the small footprint further reduces costs by enabling 2-layer PCB integration. LDOs and an LNA are built-in and costly external memory is not needed. This makes UBX G7020 positioning chips the ideal solutions for cost sensitive applications that don't require firmware update capability. For applications needing firmware update capability or taking advantage of the data logging feature the UBX-G7020 can be connected to an external SQI FLASH memory. Lower price GPS/GNSS crystals as well as high performance TCXOs are also supported.

1.2 Architecture

Figure 1 shows the block diagram of the UBX-G7020. The internal LNA requires an external input matching. As with its predecessor, u-blox 6, the customer can choose between an external TCXO and an external crystal using the internal oscillator to provide the UBX-G7020's system clock. New with u-blox 7 is the internal DC/DC converter reducing the power consumption significantly. A RTC crystal, an antenna supervisor circuit and an external SQI FLASH memory can be added optionally.

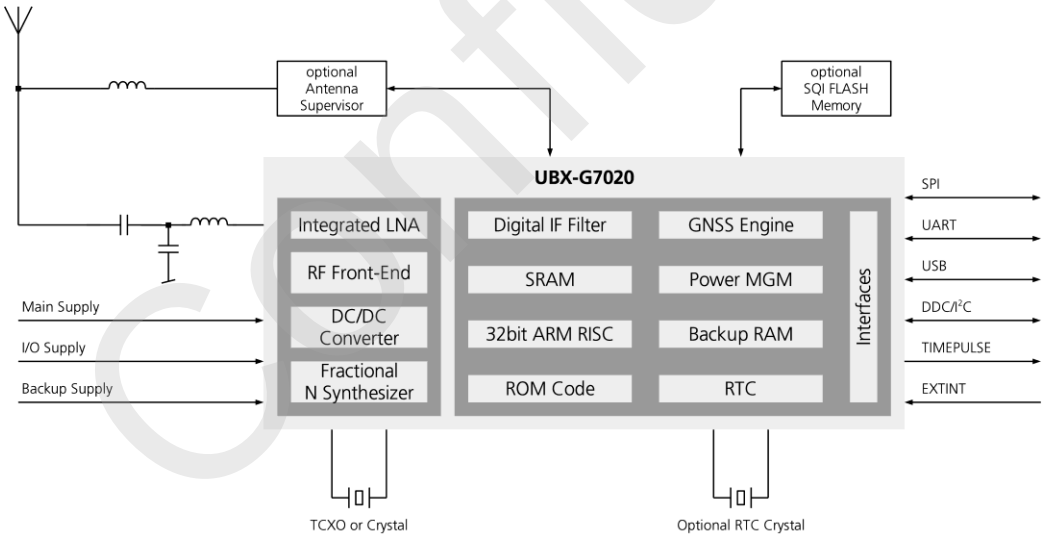


Figure 1: UBX-G7020 block diagram

2 Design-in

In order to obtain good performance with UBX-G7020 chip design, there are a number of points that require careful attention during the design-in. These include:

- Power Supply:

  Good performance requires a clean and stable power supply.
- Interfaces:

  Ensure correct wiring, rate and messages setup on the chipset and the host system.
- Antenna interface:

  For optimal performance seek short routing, matched impedance and no stubs.
- RF front-end:

  Use an external LNA if your design doesn't include an active antenna and optimal performance is important.
- Clock/ Oscillator:

  A stable clock is essential for GPS/GNSS performance.
- Configuration:

  It is mandatory for stable operation that all the configurations (Low Level Configuration) of the UBX-G7020 are set properly.

2.1 Power management

All the internal voltages for the UBX-G7020 are generated by internal LDOs. Thus no additional external LDOs are required.

Figure 2 shows typical supply scheme of the Power Management Unit of the UBX-G7020.

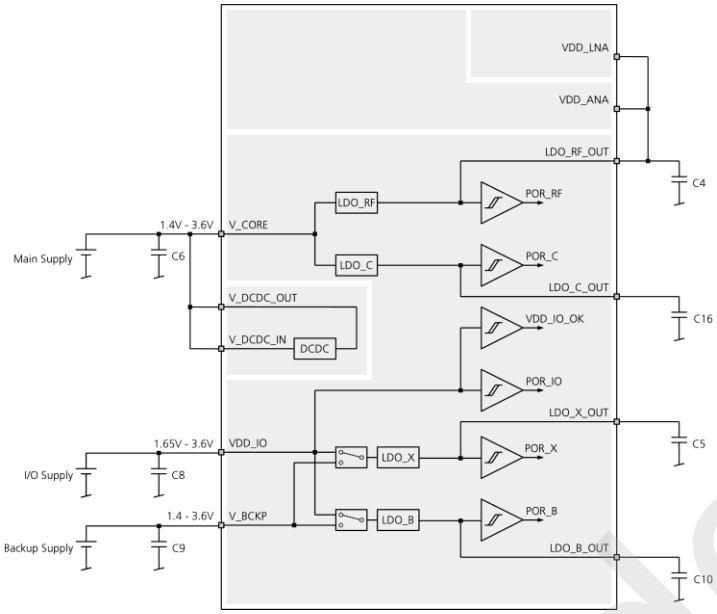


Figure 2: UBX-G7020' PMU

In addition the UBX-G7020 has an internal DC/DC converter, which optionally can be used to reduce the power consumption, see section 2.1.2.1.1. Using the DC/DC converter requires one external inductor and one external capacitor.

2.1.1 Power domains

The internal LDOs, which are LDO_B, LDO_C, LDO_RF and LDO_X, are used to provide the voltages for the 4 power domains, which are called backup, core, RF and clock domain. All the power domains are controlled by PORs (Power On Resets), which are described in section 2.1.3.

2.1.1.1 Backup domain

The voltage for the backup domain is generated by LDO_B and is either supplied by VDD_IO or in case of a power failure at VDD_IO, by V_BCKP. There is a voltage monitor at VDD_IO, VDD_IO_OK, which switches the supply for the backup domain from VDD_IO to V_BCKP in case of power failure at VDD_IO.

The control registers for the UBX-G7020 are located in the backup domain - an always on domain which means if the backup domain is not supplied, all the other domains will not be turned on. All the GPS/GNSS orbit data and time are maintained in the backup memory to which the functional configuration can also be saved. The backup domain also runs the RTC (Real Time Clock) section.

Use of valid time and the GPS/GNSS orbit data at start up will improve the GPS/GNSS performance i.e. enables Hotstarts, Warmstarts and the AssistNow Autonomous process as well as the Power Save Mode. To make use of these features connect a battery to V_BCKP to continue supplying the backup domain in case of power failure at VDD_IO.

If no backup battery is used, V_BCKP must be connected to VDD_IO.

2.1.1.2 Core domain

The voltage for the core domain is generated by LDO_C and is supplied by V_CORE. The core domain is the main digital power domain and consists of the largest blocks in the chip and sinks most of the current. When it is switched off, the RF power domain is also switched off.

The core domain requires the backup domain to be alive.

2.1.1.3 RF domain

The voltage for the RF domain is generated by LDO_RF and is supplied by V_CORE. This RF domain supplies most of the analogue RF section.

The LDO_RF_OUT is used to supply VDD_ANA and VDD_LNA.

The RF domain needs the core domain to be alive.

2.1.1.4 Clock domain

The voltage for the clock domain is generated by LDO_X and is normally supplied by VDD_IO. If the "single crystal" feature is enabled to provide the RTC function (see section RTC) and there is a power failure at VDD_IO then the LDO_X input will be switched over to V_BCKP to supply the clock domain

The LDO_X provides the supply for the oscillator and all the clock related circuits.

When a TCXO is used, the LDO_X_OUT voltage has to be used to supply or enable it. The LDO_X_OUT voltage is configurable and has to meet the TCXO power supply voltage. See section 2.4.5.

The clock power domain requires the backup domain to be alive.

☞ If a TCXO is used, LDO_X_OUT has to be used to supply or enable it.

☞ Remember to configure the LDO_X_OUT voltage according to the TCXO supply or enable voltage.

2.1.2 Supply voltages

2.1.2.1 V_Core: Main supply voltage

V_CORE is the main supply which supplies the LDO_RF and LDO_C regulators to provide voltages for the core domain and the RF domain.

The current at V_CORE depends heavily on the current system state and in general exhibits very dynamic behaviour.

☞ Do not add any series resistance (< 0.2 Ohm) into V_CORE supply as it will generate input voltage noise owing to the dynamic current conditions.

2.1.2.1.1 DC/DC converter

To improve the power consumption, the supply for V_CORE can be generated with the optional built in DCDC converter. It generates an output voltage of ~1.45V.

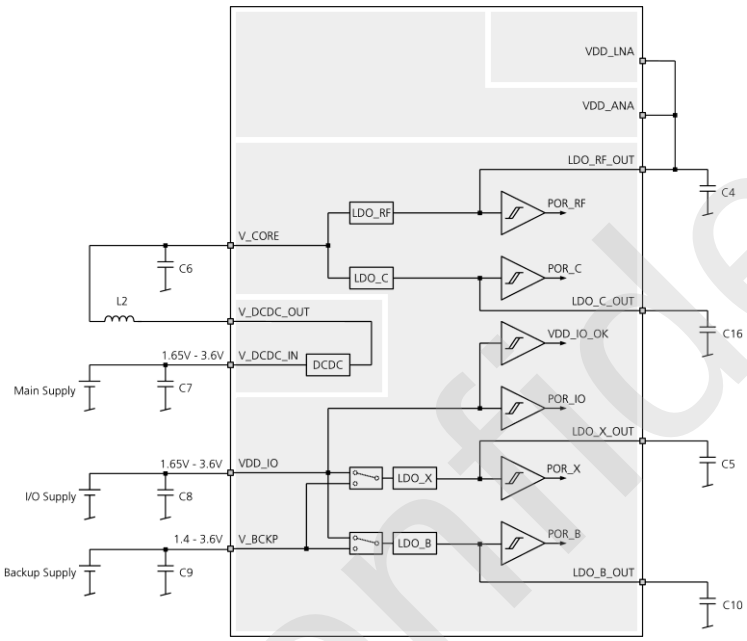


Figure 3: UBX-G7020' PMU using DCDC converter

The DC/DC block provides an energy conversion efficiency of about 85%, the actual value depending on current drawn and external inductor L2 and capacitor C6 used. Thus the power savings at a 3.3V power supply can be almost 50%, see Figure 4.

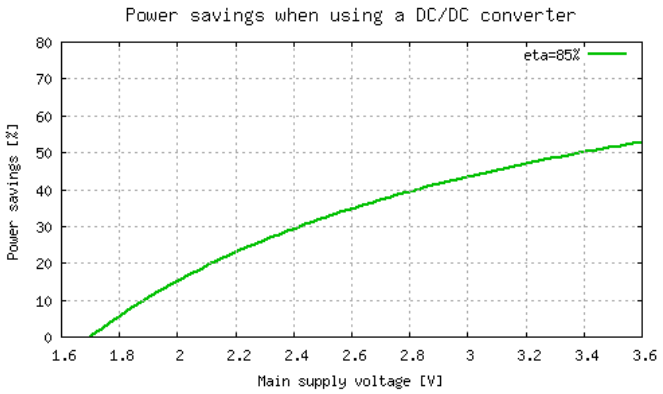


Figure 4: Power Savings using DCDC converter

For a 1.8V supply it does not make sense to use the DC/DC converter; the power savings are marginal (~5%). By default the DC/DC converter is disabled.

☞ The DC/DC converter has to be enabled by the Low Level Configuration. See section 2.10.2.

☞ If the DC/DC converter is not used, V_DCDC_IN and V_DCDC_OUT must be connected to V_CORE.

The V_DCDC_IN pin may sink short term currents of up to 400mA when the DC/DC converter is enabled and the receiver enters a Software Backup state, which can occur during Power Save Mode operation.

2.1.2.2 VDD_IO: I/O, clock and backup domain supply voltage

VDD_IO supplies all the PIOs, the backup domain and the clock domain. Thus all the PIOs comply with VDD_IO voltage levels.

The current drawn at VDD_IO depends on the activity and loading of the PIOs plus the crystal or TCXO consumption. Most of the VDD_IO current is consumed by the SQI bus if the firmware runs out of the optional SQI flash.

2.1.2.3 V_BCKP: Backup supply voltage

In the event of a power failure at VDD_IO, the backup domain will be supplied by V_BCKP. Furthermore, if the "single crystal" feature is enabled (which derives the RTC frequency from the main clock), it also supplies the clock domain in case of a power failure at VDD_IO.

Providing a V_BCKP supply will maintain the time (RTC) and the GPS/GNSS orbit data in backup memory. This ensures that any subsequent re-starts after a VDD_IO power failure will benefit from the stored data, providing a faster TTFF than otherwise possible, e.g. when performing a hotstart, warmstart of making use of the AssistNow Autonomous or AssistNow Offline functions. Thus make sure the V_BCKP supply is independent of VDD_IO supply.

The GPS satellite ephemeris data are typically valid for up to 4 hours, so it makes sense that the battery/ capacitor at V_BCKP is able to supply the backup current for at least 4 hours to enable hotstarts. For warmstarts or when making use of the AssistNow Autonomous or AssistNo Offline functions the V_BCKP source has to be able to supply current for up to a few days.

☞ If the "single crystal" feature is used, the current into V_BCKP will be increased! Make sure your backup battery capacity is chosen accordingly to meet your specification.

☞ If a backup supply is not provided connect V_BCKP to VDD_IO.

2.1.2.4 VDD_ANA and VDD_LNA

VDD_ANA is the supply for all the analogue parts in the UBX-G7020. VDD_LNA is the supply for the low noise amplifier inside the UBX-G7020.

VDD_ANA and VDD_LNA must be supplied by VDD_RF_OUT. If a clean power supply cannot be provided at V_CORE (which supplies the LDO_RF), it is recommended to add external filtering (FB1 and C3) to supply VDD_ANA/ VDD_LNA.

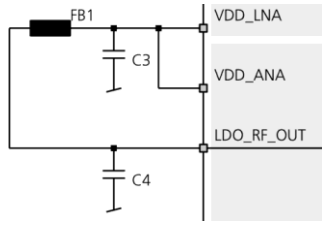


Figure 5: Filtering for VDD_LNA and VDD_ANA

2.1.3 Built in supply monitors

Built-in supply voltage monitors ensure that the system always operates in safe regions. The following conditions need to be met in order for the system to run properly:

1. The backup domain voltage LDO_B_OUT, the core domain voltage LDO_C_OUT and the RF domain voltage LDO_RF_OUT need to be within specification. These voltages are supervised by POR_C, POR_B and POR_RF.

2. The I/O voltage VDD_IO needs to be within specification. This voltage is supervised by POR_IO. This supply monitor has a configurable threshold. If external SQI flash is used the POR_IO threshold has to be set according to the power supply voltage of the SQI Flash used to ensure that the system only starts when the supply voltage for the SQI flash is reached. Otherwise, the system may fail to detect the external SQI flash and the SQI flash will be ignored.

3. The clock domain voltage LDO_X_OUT needs to be within specification. This voltage is supervised by POR_X. This supply monitor has a configurable threshold. If a TCXO is used the threshold has to be set according to the supply or enable voltage of the TCXO supplied by LDO_X_OUT.

After release of POR_C the systems waits for 2048 clock cycles to occur before the clock signal is fed into the core. This ensures system operation begins with a clean stable clock signal.

An additional supply monitor at pin VDD_IO, the VDD_IO_OK, switches the supply of the backup domain from VDD_IO to V_BCKP, once VDD_IO falls below its operational specification. Thus, a separate supply source (at V_BCKP) can be used to maintain RTC and backup RAM information even if VDD_IO fails.

2.1.4 Operating Modes

2.1.4.1 Continuous Mode

Continuous Mode uses the acquisition engine at full performance resulting in the shortest possible TTFF and the highest sensitivity. It searches for all possible satellites until the Almanac is completely downloaded. The receiver then switches to the tracking engine to reduce power consumption.

Thus, a lower tracking current consumption level will be achieved when:

- A valid position is obtained
- The entire Almanac has been downloaded
- The Ephemeris for each satellite in view is valid

☞ For best GNSS performance use Continuous Mode.

2.1.4.2 Power Save Mode

u-blox 7 GPS/ GNSS receivers include two Power Save Mode operations called ON/OFF and Cyclic tracking that allow reducing the average current consumption in different ways to match the needs of the specific application. Both operations can be set and configured by sending the corresponding UBX messages to the receiver. For more information, please see the u-blox 7 Receiver Description including Protocol Specification [3]

In Power Save Mode, the supply voltages (V_CORE and VDD_IO) must remain inside operating conditions. The system may shut down an optional external LNA by the ANT_ON signal to optimize the power consumption, see section 2.6.2.2.

☞ Use of the USB Interface is not recommended with Power Save Mode since the USB standard does not allow a device to be non-responsive and hence must be continuously active. Thus it is not possible to take full advantage of Power Save Mode operations in terms of saving current consumption.

☞ Power Save Mode requires the RTC to be maintained. This can be achieved by connecting an external RTC crystal or deriving the RTC via the main clock using the “single crystal” feature. - See section 2.5.

2.2 PIOs

There are 17 PIOs, PIO0 to PIO16, available on the UBX-G7020. All the PIOs are supplied by VDD_IO, thus all the voltage levels of the PIO pins are related to VDD_IO supply voltage. All the inputs have internal pull-up resistors in normal operation. Thus PIOs can be left open if not used.

The PIOs functions comprise the communication interfaces, antenna supervision, some configuration, the time pulse and interrupt signals.

PIO #	Default Function	I/O	Remarks	Alternative Functions
0	SQI_D0 or CFG_FFU2	I/O I	Data line 0 to external SQI FLASH or reserved configuration pin In case PIO5 is GND (no SQI flash used) it acts as a reserved configuration pin	
1	SQI_D1 or CFG_DCDC	I/O I	Data line 1 to external SQI FLASH or configuration pin In case PIO5 is GND (no SQI flash used) it acts as a configuration pin to enable DCDC converter	
2	SQI_D2 or CFG_OSC3	I/O I	Data line 2 to external SQI FLASH or configuration pin In case PIO5 is GND (no SQI flash used) it acts as an oscillator configuration pin	
3	SQI_D3 or CFG_OSC2	I/O I	Data line 3 to external SQI FLASH or configuration pin In case PIO5 is GND (no SQI flash used) it acts as an oscillator configuration pin	
4	SQI_CLK or CFG_OSC1	O I	Clock for external SQI FLASH or configuration pin In case PIO5 is GND (no SQI flash used) it acts as an oscillator configuration pin	
5	SQI_CS or CONFIG_SEL	I/O I	Chip select for external SQI FLASH or configuration enable pin If low at startup (no SQI flash used) PIO0 to PIO4 become configuration pins	
6	TX or MISO	O O	UART TX or SPI MISO Depends on PIO10 (D_SEL) status	TX-ready
7	RX or MOSI	I I	UART RX or SPI MOSI Depends on PIO10 (D_SEL) status	
8	SCL or SCK	O O	DDC clock or SPI clock Depends on PIO10 (D_SEL) status	
9	SDA or CS_N	I/O O	DDC data or SPI chip select Depends on PIO10 (D_SEL) status	
10	D_SEL	I	Communication interface selection pin Selects the communication interface available on PIO6 to PIO9	
11	TIMEPULSE1	O	Time pulse 1 output, 1pps	
12	SAFEBOOT_N	I	If low at startup the receiver will start in Safe Boot Mode. Used in production for setting the Low Level Configuration, programming the SQI flash and testing purposes.	TIMEPULSE2
13	-	I	No function by default, leave open	EXTINT0, TX-ready
14	-	I	No function by default, leave open	EXTINT1, ANT_DET, TX-ready
15	ANT_OK	I	Antenna status of antenna supervisor	ANT_SHORT_N, UART_TX, TX-ready
16	ANT_OFF	O	Antenna power control of antenna supervisor	UART_RX, TX-ready

Table 1: PIO overview

2.2.1 SQI Flash memory

An SQI (Serial Quad Interface) flash memory can be connected to the SQI interface (PIO0–PIO5) to provide the following options:

- Run firmware out of the SQI flash and have the possibility to update the firmware
- Save data logging results
- Store the Functional Configuration permanently
- Save the Low Level Configuration (system configuration)
- Hold AssistNow Offline data

☞ If updating of the firmware is a prime requirement then an SQI flash must be connected.

☞ Some UBX-G7020 features may be only available with a particular Flash Firmware.

The voltage level of the SQI interface follows the VDD_IO level. Thus make sure the SQI Flash is supplied with the same voltage as VDD_IO of the UBX-G7020. It is recommended to place a decoupling capacitor (C2) close to the supply pin of the SQI flash.

☞ Make sure that the SQI Flash supply range matches the voltage supplied at VDD_IO.

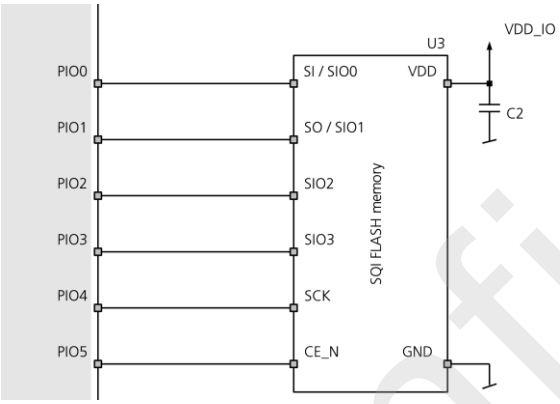


Figure 6: Connecting a SQI FLASH memory

Not all the SQI flash devices supported by the UBX-G7020 can be used to do logging, see section 3.4.

To run the firmware out of the SQI flash a minimum size of 4Mb is required. A 4Mb device is also sufficient to save AssistNow Offline information plus the Low Level Configuration and functional configuration data. However, to run Firmware from the SQI flash and provide space for logging results, a minimal size of 8Mb is required. If, on the other hand the SQI flash is just used for logging results and the firmware runs out of ROM, a 4Mb SQI flash can provide reasonable space for logged data.

For a list of supported SQI Flash devices please see Table 19.

There is a configurable VDD_IO monitor threshold (POR_IO) to ensure that the UBX-G7020 only starts if the VDD_IO supply (which is used to supply the SQI flash), is within the supply range of the SQI flash device. This will ensure that any connected Flash memory will be detected correctly at startup.

☞ The VDD_IO monitor threshold (POR_IO) must be set according to the SQI supply voltage level (VDD_IO) in the eFuse by the Low Level Configuration, see section 2.10.2!

Place the SQI FLASH close to the UBX-G7020 chip to keep the interface lines short and if possible route them on inner layers to avoid noise emission. Also make sure that all the lines are not too-long/ too-thick to reduce capacitance/ time delays.

At initial start up in production, the UBX-G7020 will not have information about the supply voltage or oscillator settings required and hence may not be able to start up without this information. Hence an initial power-up requires starting in Safe Boot Mode in which the receiver runs from an internal ring oscillator. Then the Low Level Configuration can be set in the eFuse or in the SQI flash. See section 2.2.6 and section 2.10.2.

☞ Make sure the SAFEBOOT_N pin (PIO12) is made available to enter the Safe Boot Mode, a pre-requisite to program the flash and preset the Low Level Configuration in production.

2.2.2 Configuration pins

If no SQI flash is connected, there is a configuration enabling pin (PIO5) which activates 5 configuration pins PIO0 to PIO4. These pins allow setting some essential oscillator and power supply (DCDC converter) configurations.

☞ PIO5 connected to GND will enable configuration pins at PIO0 to PIO4!

PIO0 is reserved and must be left open when no SQI Flash is employed.

All the configuration pins have internal pull-ups. Any left open equates to a logical "1".

PIO5	Configuration	Remarks
1 (open)	Configuration pins disabled	The configuration done by PIO0 to PIO4 is ignored.
0 (GND)	Configuration pins **enabled**	

Table 2: Enable configuration pins

PIO1	Configuration	Remarks
1 (open)	DCDC converter disabled	
0 (GND)	DCDC converter enabled	Requires additional circuitry

Table 3: DCDC converter configuration pin

PIO2	PIO3	PIO4	Configuration	Remarks
1 (open)	**1** (open)	**1** (open)	Crystal 19pF load	
0 (GND)	**1** (open)	**1** (open)	Reserved	
1 (open)	**0** (GND)	**1** (open)	Reserved	
0 (GND)	**0** (GND)	**1** (open)	Reserved	
1 (open)	**1** (open)	**0** (GND)	LDO_X_OUT = 3.01V	LDO_X_OUT supplies and enables the 3V TCXO.
0 (GND)	**1** (open)	**0** (GND)	LDO_X_OUT = 1.91V	LDO_X_OUT supplies and enables the 1.8V TCXO.
1 (open)	**0** (GND)	**0** (GND)	LDO_X_OUT = 2.69V	LDO_X_OUT used to enable the 3V TCXO; TCXO supplied directly by same voltage as used to supply VDD_IO.
0 (GND)	**0** (GND)	**0** (GND)	LDO_X_OUT = 1.67V	LDO_X_OUT used to enable the 1.8V TCXO; TCXO supplied directly by same voltage as used to supply VDD_IO.

Table 4: Oscillator configuration pins

☞ For oscillator circuits and recommendations see section 2.4!

☞ PIO0 is reserved for further use. Leave it open.

For further information about the Low Level Configuration of the UBX-G7020 see section 2.10.2.

2.2.3 Communication interfaces

A UART, SPI and DDC (I^2C compatible) interface is available to communicate with a host on the UBX-G7020. There is also a USB interface available on dedicated pins, see section 2.7.

The UART, SPI and DDC pins are supplied by and operate at VDD_IO voltage levels.

There are 4 pins (PIO6 to PIO9) to provide a UART, DDC and SPI interface for communication with a host CPU. These 4 PIOs can be configured as either 1 x UART and 1 x DDC or a single SPI interface selectable by the PIO10 (D-SEL pin). Table 5 below provides the port mapping details.

If the SPI port is used for communication to a host CPU, there is the possibility to configure the UBX-G7020 so that the UART is mapped to PIO15 and PIO16. Thus the UART can be used as a debug interface or a second communication interface if needed. To remap the UART use the Low Level Configuration, see section 2.10.2 and u-blox 7 Receiver Description including Protocol Specification [3].

PIO #	PIO10 (D_SEL) = "high" (left open)	PIO10 (D_SEL) = "Low" (connected to GND)	PIO10 (D_SEL) = "Low" (connected to GND) and UART remapped
PIO6	UART TX	SPI MISO	SPI MISO
PIO7	UART RX	SPI MOSI	SPI MOSI
PIO8	DDC SCL	SPI CLK	SPI CLK
PIO9	DDC SDA	SPI CS	SPI CS
PIO15	ANT_OK	ANT_OK	UART TX
PIO16	ANT_OFF	ANT_OFF	UART RX

Table 5: Communication Interfaces overview

☞ It is not possible to have both the DDC and SPI interfaces active simultaneously for communication with a host.

☞ For debugging purposes it is recommended to have a second interface independent from the application available via test-points.

☞ The optional remapped UART interface is not available in Safe Boot Mode, see section 2.2.6.

For each interface, a dedicated pin can be defined to indicate that data is ready to be transmitted. This Tx-ready pin can be mapped to any unused PIO pin. Each Tx-ready pin is associated with a particular interface and cannot be shared. If the nominated PIO has another function by default, it needs to be disabled before configuring the Tx-ready signal to that PIO pin. For configuration of the Tx-ready feature see u-blox 7 Receiver Description including Protocol Specification [3].

2.2.3.1 UART interface

A UART interface is available for serial communication to a host CPU. The UART interface supports configurable data rates of which the default is 9600 baud. The signals levels are related to VDD_IO supply voltage. An interface based on RS232 standard levels (+/- 7 V) can be realized using level shifter ICs such as the Maxim MAX3232.

Hardware handshake signals and synchronous operation are not supported.

A signal change on the UART RX pin can also be used to wake up the receiver in Power Save Mode (see u-blox 7 Receiver Description including Protocol Specification [3].).

☞ The UART can be permanently remapped by Low Level Configuration to PIO15 and PIO16, see section 2.10.2.

2.2.3.2 Display Data Channel (DDC) Interface

An I²C compatible Display Data Channel (DDC) interface is available for serial communication with a host CPU.

The PIO8 (SCL) and PIO9 (SDA) pins have internal pull-up resistors sufficient for most applications. However, depends on the speed of the host and the load on the DDC lines it might happen that additional external pull-up resistors are necessary.

☞ To make use of DDC interface the PIO10 (D_SEL) has to be left open.

☞ The UBX-G7020 DDC interface provides serial communication with u-blox LEON-G100/G200 wireless modules from version LEON-G100/G200-05S and above and on all LISA modules.

☞ The TX-ready feature is supported on version LEON FW 7.xx and LISA-U2 01S and above.

For more information about DDC implementation refer to the u-blox 7 Receiver Description including Protocol Specification [3].

2.2.3.3 SPI Interface

The SPI port provides a serial communication interface with a host CPU.

☞ To make use of the SPI interface, PIO10 (D_SEL) has to be connected to GND.

2.2.3.4 Electromagnetic interference on interface signal lines

Any interface signal line (length > ~3 mm) may pick up high frequency signals and transfer this noise into the GPS/GNSS receiver. This specifically applies to unshielded lines, lines were the corresponding GND layer is remote or missing entirely, and lines close to the edges of the printed circuit board. If a GSM signal radiates into an unshielded high-impedance line, noise in the order of Volts can be generated and eventually not only distort receiver operation but also damage it permanently.

In such case it is recommended to use feed-thru capacitors with a good GND connection close to the GPS/GNSS receiver in order to filter such high-frequency noise. See Section 3.19 for component recommendations. Alternatively, ferrite beads (see Section 3.18) can be used. These work without GND connection but may adversely affect signal rise time.

EMI protection measures are recommended when RF emitting devices are near the GPS/GNSS receiver. To minimize the effect of EMI a robust grounding concept is essential. To achieve electromagnetic robustness follow the standard EMI suppression techniques. Some references are provided in [4] and [5].

2.2.4 Time pulse

There are 2 configurable time pulse output signals available with the UBX-G7020 chip; TIMEPULSE1 and TIMEPULSE2. These two time pulse signals can only run on PIO11 and PIO12. By default only TIMEPULSE1 on PIO11 is enabled and outputs a 1PPS signal.

The PIO12 is also used as the SAFEBOOT_N pin at start up, which is needed to enter the Safe Boot Mode, see 2.2.6.

For further information see u-blox 7 Receiver description including protocol specification [3].

2.2.5 External interrupt

There are 2 configurable external interrupt inputs available with the UBX-G7020 chip; EXTINT0 and EXTINT1 available at PIO13 and PIO14 respectively. By default both external interrupts, EXTINT0 and EXTINT1, are disabled.

External Interrupts can be used for:

- Wake-up in Power Save Mode.
- For time mark aiding.
- For frequency aiding.
- For on/off control of the GPS/GNSS receiver

For further information see u-blox 7 Receiver description including protocol specification [3].

☞ If the EXTINT pin is configured for on/off switching of the UBX-G7020 chip, the internal pull-up becomes disabled. Thus make sure the EXTINT input is always driven within the defined voltage level by the host.

2.2.6 SAFEBOOT_N Pin/ Safe Boot Mode

PIO12 is the SAFEBOOT_N pin. If this pin is "low" at start up, the UBX-G7020 will start up in Safe Boot Mode and will not enter GPS/GNSS operation. In Safe Boot Mode the UBX-G7020 runs from an internal ring oscillator and starts regardless of any configuration provided by the configuration pins or configuration saved in SQI flash. Thus it can be used to recover from a situation where the SQI flash was corrupted or programmed with incorrect Low Level Configuration settings.

Owing to the inaccurate frequency of the internal ring oscillator the UBX-G7020 is unable to communicate by USB in Safe Boot Mode! For communication by UART in Safe Boot Mode a training sequence can be sent by the host to the UBX-G7020 in order to enable communication. For further information see u-blox 7 Receiver description including protocol specification [3]. The optional remapped UART interface is not available in Safe Boot Mode.

Safe Boot Mode is used in production to program the SQI FLASH and to set the Low Level Configuration in the eFuse or in the SQI flash.

It is recommended to have the possibility to pull the SAFEBOOT_N pin "low" at startup of the UBX-G7020. This can be provided using an externally connected test point or via a host CPUs digital I/O port.

☞ The UBX-G7020 is not able to communicate by USB in Safe Boot Mode.

☞ All UBX-G7020 designs using SQI flash which do not use the default settings regarding oscillator, e.g. 26MHz crystal with 19pF load capacitance must be able to enter the Safe Boot Mode at production to set the Low Level Configuration and program the SQI flash!

2.2.7 Active Antenna Supervisor

u-blox 7 firmware supports active antenna supervisors. There is either a 2-pin or a 3-pin antenna supervisor. By default the 2-pin antenna supervisor is enabled. The antenna supervisor pins are located at PIO14, PIO15 and PIO16.

☞ If the UART is remapped to PIO15 and PIO16, the antenna supervisor cannot be used!

The antenna supervisor gives information about the status of the active antenna and will turn off the supply to the active antenna in case a short is detected or to optimize the power consumption when in Power Save Mode.

2.2.7.1 2-pin antenna supervisor

The 2-pin antenna supervisor function, which is enabled by default, comprises PIO15 for the ANT_OK input and PIO16 for the ANT_OFF output.

PIO #	Function	I/O	Description	Remarks
PIO15	ANT_OK	I	Antenna OK "high" = Antenna OK "low" = Antenna not OK	Polarity can be changed by Low Level Configuration if the external circuitry requires other polarity, see section 2.10.2
PIO16	ANT_OFF	O	Control signal to turn on and off the antenna supply "high" = Antenna OFF "low" = Antenna ON	Polarity can be changed by Low Level Configuration if the external circuitry requires other polarity, see section 2.10.2

Table 6: 2-pin antenna supervisor pins

The circuitry as shown in Figure 7 provides antenna supply short circuit detection. It will prevent antenna operation via transistor T1 if a short circuit has been detected or if it is not required (e.g. in Power Save Mode).

The status of the active antenna can be checked by UBX-MON-HW message. See the u-blox 7 Receiver Description including Protocol Specification [3].

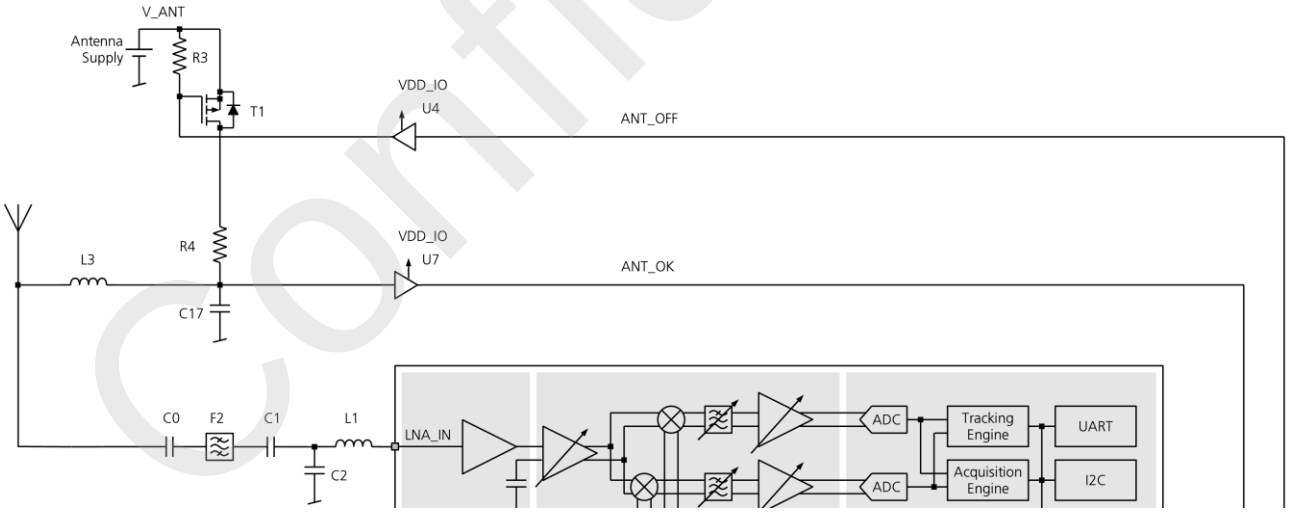


Figure 7: 2-pin Antenna Supervisor

If the antenna supply voltage V_ANT exceeds VDD_IO, open drain buffers U4 and U7 (e.g. Fairchild NC7WZ07) are needed to shift the voltage levels. R3 is required as a passive pull-up to control T1 because U4 has an open drain output. R4 serves as a current limiter in the event of a short circuit.

2.2.7.2 3-pin antenna supervisor

The 3-pin antenna supervisor comprises pin PIO14 for ANT_DET (active antenna detection), PIO15 for ANT_SHORT_N (short detection) and PIO16 for ANT_OFF (antenna on/off control). This function must be enabled by Low Level Configuration.

PIO #	Function	I/O	Description	Remarks
PIO14	ANT_DET	I (pull-up)	Antenna detected "high" = Antenna detected "low" = Antenna not detected	Polarity can be changed by Low Level Configuration if the external circuitry requires other polarity, see section 2.10.2
PIO15	ANT_SHORT_N	I (pull-up)	Antenna not shorted "high" = antenna has no short "low" = antenna has a short	Polarity can be changed by Low Level Configuration if the external circuitry requires other polarity, see section 2.10.2
PIO16	ANT_OFF	O	Control signal to turn on and off the antenna supply "high" = turn off antenna supply "low" = short to GND	Polarity can be changed by Low Level Configuration if the external circuitry requires other polarity, see section 2.10.2

Table 7: 3-pin Antenna supervisor pins

The external circuitry as shown in Figure 8 provides detection of an active antenna connection status. i.e. if it is present the DC supply current exceeds a preset threshold defined by R4, R5, and R6 It will shut down the antenna via transistor T1 if a short circuit has been detected via U7 or if it's not required (e.g. in Power Save Mode).

The status of the active antenna can be checked by UBX-MON-HW message. See the u-blox 7 Receiver Description including Protocol Specification [3].

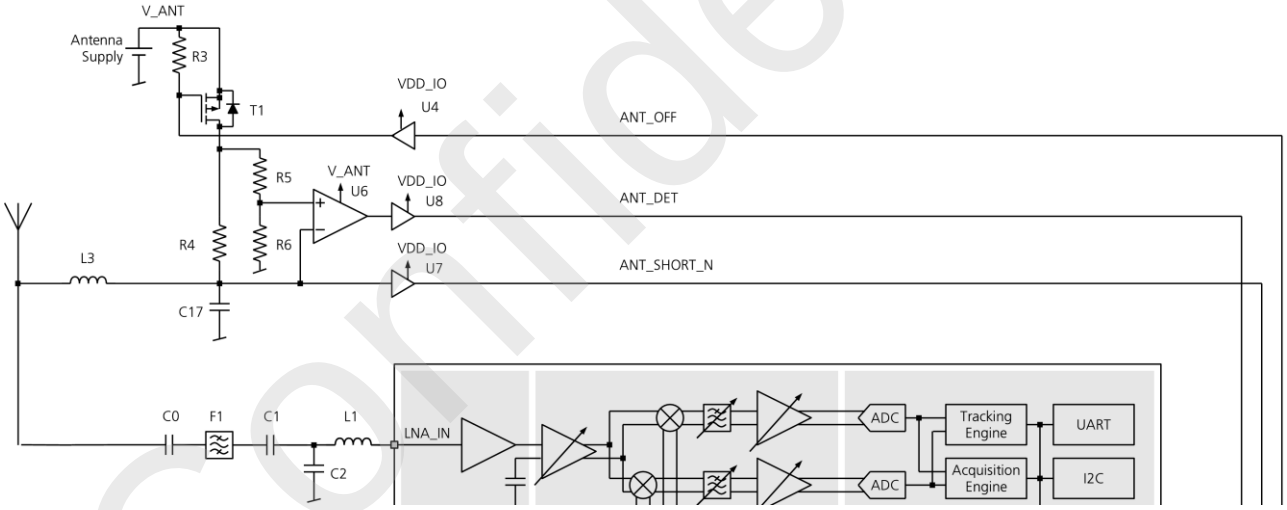


Figure 8: 3-pin Antenna Supervisor

If the antenna supply voltage V_ANT exceeds VDD_IO, the open drain buffers U4, U7 and U8 (e.g. Fairchild NC7WZ07) are needed to shift the voltage levels. R3 is required as a passive pull-up to control T1 because U4 has an open drain output. R4 serves as a current limiter in the event of a short circuit.

2.3 System reset

The UBX-G7020 provides a RESET_N pin to reset the system. The RESET_N is an edge triggered input only pin with an internal pull-up resistor. It is used to reset the system without affecting the temporary GNSS/GPS data saved in the backup memory. Thus AssistNow Autonomous data, time information and ephemeris will still be available. Leave RESET_N open for normal operation. The RESET_N complies with the VDD_IO level and can even be driven high actively.

☞ In the reset state the UBX-G7020 consumes significant amount of current, thus it is recommended to use the RESET_N only with a reset signal, not as an enable/disable pin.

2.4 Clock generation

The UBX-G7020 can be clocked either by a TCXO or by a crystal using the internal oscillator. The crystal oscillator option represents a low-cost solution where signal acquisition times are typically extended in case of weak signals. A TCXO is more expensive but provides better performance and is easier to integrate. The UBX-G7020 has to be configured by the Low Level Configuration regarding the choice of the frequency source, see section 2.10.2.

☞ A stable and clean clock is the key for good GPS/GNSS performance.

The following tips are helpful for establishing a stable and clean clock:

- A stable VDD_IO supply voltage, which supplies in certain cases the TXCO the LDO_X for the clock domain.
- No air convection or fast temperature changes at the TCXO or crystal is essential - cover the TCXO or crystal with a shield and place the TCXO or crystal in a temperature stable area e.g. far away from a fan or power consuming ICs. If the TCXO or crystal has to be placed close to the UBX-G7020 chip, make use of the internal DC/DC converter option to minimize the power consumption of the UBX-G7020 chip to lower the impact of temperature gradients to the oscillator performance.
- Use only appropriate TCXOs or crystals, which are intended for GPS applications, see sections 3.1 and 3.2. This ensures that they are tested to reject frequency jumps and perturbations when temperature cycled.

2.4.1 Clock accuracies and tolerances

The GPS/GNSS crystal or TCXO reference frequency behavior is essential for the overall GPS/GNSS system performance. To enable fast weak signal acquisition, tolerances on the crystal specifications have to be tightened. This leads to the requirement of a TCXO instead of an ordinary crystal.

Tolerances	TCXO	Crystal
Calibration (Initial) Tolerance [+/-ppm]	2	7
Temperature Tolerance [+/-ppm]	0.5	15
Aging after 10 years [+/-ppm]	4	5
Total [+/-ppm]	**6.5**	**27**

Table 8: Tolerance Specifications for clock frequency

The UBX-G7020 continuously stores crystal/TCXO calibration values in the backup RAM as long as a backup voltage (V_BCKP) is available. This allows more accurate compensation for initial TCXO or crystal frequency offsets when re-starting.

Correct specification of the clock source has two main effects on GPS/GNSS firmware performance:

1. For a cold start scenario the maximum total tolerance as summed up in Table 8 defines the maximum frequency search span. If the actual frequency error of the UBX-G7020 clock source is larger than indicated by the system configuration, the signal may never be found.

2. For aided or hot start scenarios the temperature tolerance is crucial. It is also important that the information about the actual calibration error (including aging) is available. This is most easily accomplished by keeping the backup RAM (in backup domain) alive. If no signal is found the frequency search space is subsequently widened up to the maximum search span used in cold start.

In any case, a frequency search always starts with the assumption of zero reference frequency error and subsequently widens the frequency search span up to the configured maximum. The closer the reference frequency is to its nominal value, the faster will a search deliver its results.

2.4.2 Crystal or TCXO package selection

Of course, the package of the crystal or TCXO can be freely chosen. However, the general rule applies that smaller packages make it more difficult to manufacture good GPS crystals. Smaller packages also have a smaller thermal mass, making them more sensitive to thermally induced frequency perturbations. SMD packages usually have a low thermal resistance to the circuit board. Temperature changes of the board, e.g. due to variation in power consumption of the UBX-G7020 or other adjacent components, may directly affect crystal/TCXO temperature. Through-hole mounted crystals are better isolated from these effects.

2.4.3 Frequency perturbations

Frequency perturbations, i.e. small frequency errors typically induced by temperature changes or changes in the drive level, will have a significant effect on GPS/GNSS performance. While the normal smooth dependency of the crystal frequency on temperature and drive level is easily compensated by GPS/GNSS firmware, a sudden discontinuity cannot be compensated for. If such perturbations occur the receiver will not be able to maintain carrier lock and will be unable to demodulate data from the satellite signal. Hence the receiver will never be able to calculate a position unless it is used with Assisted-GPS/GNSS.

Besides environmental influences such as forced air convection, poor quality of the crystal oscillator is the main source for such perturbation problems.

☞ The GPS Crystal/TCXO must be isolated from external temperature changes as well as possible. Forced air convection currents must never reach the crystal/TCXO. Temperature changes of the circuit board and thermal cycling of the system should be kept to an absolute minimum. This even holds for a TCXO because its temperature compensation feedback loop is unable to track rapid temperature changes.

Poor quality of the crystal results in excitation of unwanted oscillation modes. There are many different types of modes that can be excited during resonance apart from the desired thickness shear mode. Coupled modes, often referred to as “activity dips”, occur when two or more excited modes, or normally their harmonics, beat together. Face-shear, flexure, thickness-twist and many other modes with their respective harmonics, can couple into the main mode at a particular temperature and reduce the Q-factor and selectivity of the crystal - hence the term “activity dip”. Accompanying the activity dip is a frequency deviation from the smooth temperature characteristic curve. As well as a large frequency change, the resistance change can prevent oscillation in extreme cases. These dips are much more common with fundamental frequency modes and where the diameter or size of the crystal is small.

Crystal manufacturers can minimize the occurrence of these dips by optimizing the crystal design, however to eliminate them in production is virtually impossible. Even the best crystal designs will leave some percentage of units with dips. To ensure crystals with unwanted modes are not released requires individual unit testing. Testing the units in an environmental chamber over the operating temperature range and looking for frequency perturbations is the most effective method. Some activity dips can occur over a very narrow temperature span and will produce the worst effect. Hence the measurement resolution of the screening system is of prime importance as dips can be easily missed.

It is extremely important that the crystal does not cause any sudden jumps in phase or frequency when used in a GPS/GNSS oscillator circuit. If they occur, these frequency perturbations will cause velocity errors initially and ultimately tracking lock loss.

It has been shown that insufficient cleaning of the crystal, surface voids, or badly placed electrodes are the chief causes of poor crystal performance.

☞ When selecting a supplier for GPS/GNSS TCXOs or crystals, one should make sure that the supplier is aware of the requirements of the GPS/GNSS application. Specifically, the supplier should be able to offer a screening process targeted at elimination of activity dips or frequency perturbations with a sufficiently fine temperature step.

Crystals and TCXOs listed in Sections 3.1 and 3.2 have been found to work well in GPS/GNSS applications.

2.4.4 Crystal oscillator

The UBX-G7020 chip comes with a Pierce oscillator. It supports 26MHz crystals with 19pF load capacitance.

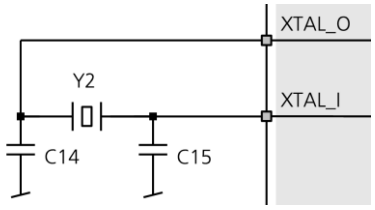


Figure 9: Crystal circuit

2.4.4.1 Crystal oscillator frequency tuning

The actual frequency of a crystal oscillator depends on its load capacitance which is mainly formed by the two capacitors C14 and C15 shown in Figure 9. Each capacitor has an additional parasitic capacitance to GND in parallel formed by the circuit traces on the printed circuit board and the capacitance of the UBX-G7020 input- and output (XTAL_I and XTAL_O). The crystal oscillator will oscillate on its specified frequency only if the crystal "sees" the specified load capacitance into the oscillator circuit (item 2.1 in Table 15). Figure 10 shows the crystal oscillator including its parasitic capacitors. Generally C14 and C15 should be equal in size, but sometimes one or two E-series steps difference in value may be required to approach the desired load capacitance.

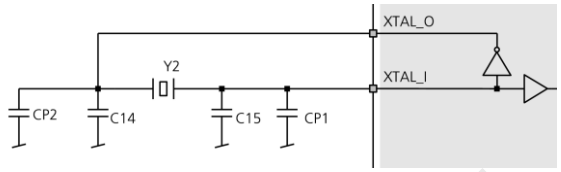


Figure 10: Crystal oscillator and parasitic capacitors

The load capacitance CL "seen" by the crystal can now be calculated as follows:

$$CL = \frac{(CP2+C14) * (CP1+C15)}{(CP2+C14) + (CP1+C15)}$$

The relation between actual frequency offset and load capacitance offset is given by the Pullability of a crystal (item 2.3 in Table 15). Generally it can be said that a crystal designed for high load capacitance will have a lower Pullability value than one designed for a lower load capacitance. However, high load capacitance values require higher power for the oscillator to operate. From the Pullability specification of the crystal used it can immediately be concluded that even a 1 pF error in load capacitance will result in a significant frequency error.

☞ Only high-quality, low-tolerance COG capacitors must be used for C14 and C15.

As it is usually quite difficult to predict circuit board parasitics accurately, it is recommended to use a tuning approach based on measurement for determination of the correct values of C14 and C15 for any given board design. The goal of the tuning is to achieve a frequency error of less than +/- 12 ppm (+/- 19 kHz Doppler) at room temperature for all produced devices.

A conventional temperature compensated crystal will also exhibit a frequency/temperature dependency. Luckily this offset is minimal at room temperature. Thus, a measurement at room temperature can be used to determine the initial offset of the oscillator circuit caused by any load capacitance error.

As it happens a GPS/GNSS receiver is also a very precise tool to measure frequencies, so not even a frequency counter is needed for this task. See the u-blox 7 Receiver Description including Protocol Specification [3] for more information about protocol messages dealing with local oscillator frequency measurements. Two options exist for the frequency measurement:

1. Using a GPS/GNSS live signal: Observe the Clock Drift value inside the UBX-NAV-CLOCK message after the receiver has acquired a position. Its measurement unit is µs/s which is actually the same as ppm.
2. Using a 1-channel simulator: Observe the Doppler value inside the UBX-MON-PT message. The crystal offset in ppm can be calculated by dividing this value by -1575.42 Hz (observe the change in sign).

The following tuning sequence is recommended:

1. Produce a few sample boards using the starting values for C14 and C15 as provided in Table 34.
2. Check frequency offset of theses samples using any of the methods mentioned above.
3. Gently change load capacitor values (increase for lower frequency) until frequency error is minimized.
4. Using the new values, start pre-series production and observe frequency offset at room temperature
5. If necessary, adjust capacitor values again.

Initial frequency tolerance of a crystal tends to show low variation across single crystal production lots. This means that one production lot (several 1000 pieces) can be well centered at 0 ppm offset, while for example the next lot can come at +5 ppm offset in average. It is therefore highly recommended to monitor crystal frequency offset continuously in production.

2.4.5 TCXO

The LDO_X_OUT, the clock domain voltage, is used to supply or supervise (enable) the TCXO. Thus it will be supervised and switched on and off by the firmware, e.g. in Power Save Mode. Any voltage ripple at VDD_IO, which supplies the LDO_X to generate LDO_X_OUT, is rejected significantly if using LDO_X_OUT to supply a TCXO. The correct LDO_X_OUT voltage has to be set by Low Level Configuration.

☞ The LDO_X_OUT voltage has to be set by the Low Level Configuration to ensure it matches the supply voltage range of TCXO! See section 2.10.2.

There are 4 main options when connecting a TCXO; each depends on the VDD_IO voltage and the supply voltage range of the chosen TCXO. The supply voltage for VDD_IO has to be chosen dependant on the voltage level needed at the PIO's to supply e.g. the communication interface, SQI interface etc. Hence the following table gives information on the configuration and circuit to be used for a given VDD_IO supply voltage and TCXO supply range combination.

Option	VDD_IO supply	TCXO used	LDO_X_OUT voltage set by config	Usage of LDO_X_OUT	Circuit	Remarks
1	2.0…3.6V	1.8V	1.9V	Supply and enable of TCXO	Figure 11	Recommended circuit.
2	3.1…3.6V	3V	3.0V	Supply and enable of TCXO	Figure 11	
3	1.65…2.0V	1.8V	1.7V	Enable of TCXO	Figure 12	Supply voltage for VDD_IO has to be used to supply TCXO. Make sure it is a very clean and stable voltage.
4	2.7…3.0V	3V	2.7V	Enable of TCXO	Figure 12	Supply voltage for VDD_IO has to be used to supply TCXO. Make sure it is a very clean and stable voltage.

Table 9: Options to supply the TCXO

A clean and stable supply voltage is essential for the performance of the TXCO and thus for the GPS/GNSS performance! So it is recommended to make use of the internal LDO_X regulator to supply the TCXO. If the LDO_X_OUT voltage is used only to supervise (enable) the TCXO, make sure a clean and stable voltage is supplied to the TCXO.

☞ A higher voltage drop at LDO_X will improve the ripple rejection from VDD_IO to LDO_X_OUT. Thus it is recommended to use a 1.8V TCXO in 3V designs; option 1 in Table 9!

If a 1.8V VDD_IO supply is used in conjunction with a 1.8V TCXO, the TCXO must not be supplied by LDO_X_OUT. Instead the TCXO has to be supplied directly from VDD_IO, LDO_X_OUT is used to enable and disable the TCXO respectively.

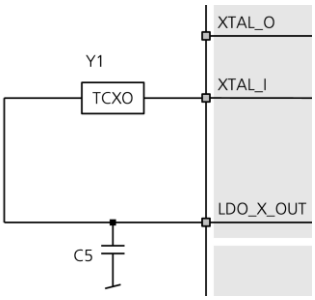


Figure 11: TCXO supplied and enabled by LDO_X_OUT

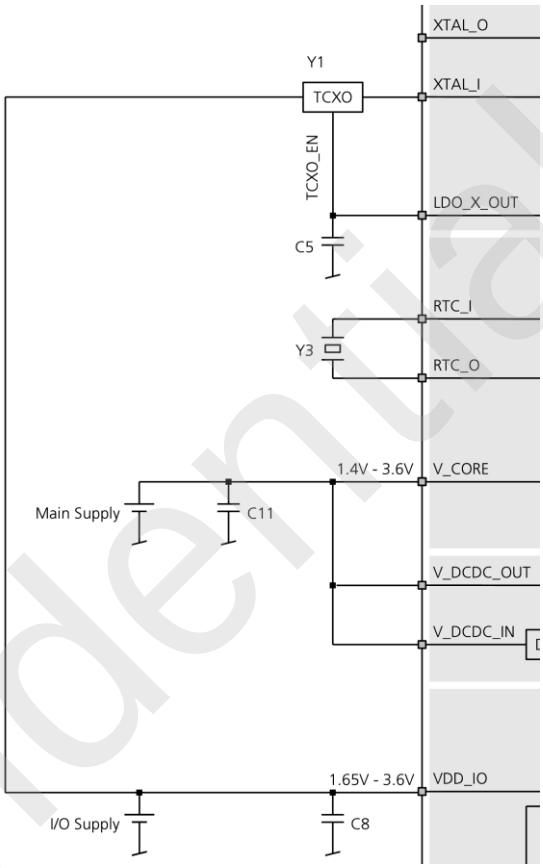


Figure 12: TCXO supplied by VDD_IO and enabled by LDO_X_OUT

2.5 Real-Time Clock (RTC)

The RTC section is located in the backup domain of the UBX-G7020. It is used to maintain time in the event of power failure at main supply, VDD_IO. The RTC is required for Hotstart, Warmstart, AssistNow Autonomous, AssistNow Offline and in some Power Save Mode operations.

The time information can either be generated by connecting an external crystal to the RTC oscillator, by deriving the RTC from the system clock, by connecting an external 32.768 kHz signal to the RTC input or by time aiding of the GPS receiver at every startup.

2.5.1 RTC using a crystal

The easiest way to provide time information to the receiver is to connect a RTC crystal to the corresponding pins of the RTC oscillator, RTC_I and RTC_O. There is no need for adding load capacitors to the crystal for frequency tuning, because they are already integrated into the UBX-G7020. Using a RTC crystal will provide lowest current consumption into V_BCKP in case a power failure. On the other hand it will increase the BOM costs and requires space for the RTC crystal.

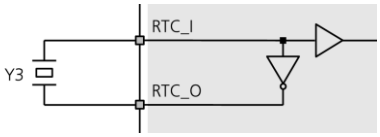


Figure 13: RTC crystal

2.5.2 RTC derived from the system clock; "Single Crystal" Feature

The UBX-G7020 can be configured by Low Level Configuration, section 2.10.2, in such way that the reference frequency for the RTC is internally derived from the TCXO or XTO system clock frequency (26MHz). This feature is called "single crystal" operation. In addition, the TCXO or XTO (see section 2.4) will be supplied by the backup battery at V_BCKP in the event of a power failure at VDD_IO. Consequently, the power consumption into V_BCKP is higher compared to the usage of an ordinary RTC crystal. On the other hand it requires less space and saves cost, owing to a smaller BOM.

For this feature RTC_I must be connected to ground and RTC_O left open. The capacity of the backup battery at V_BCKP must be dimensioned accordingly, taking account of the higher than normal current consumption at V_BCKP in the event of power failure at VDD_IO.

2.5.3 RTC using an external clock

Some applications can provide a suitable 32.768 kHz external reference to drive the UBX-G7020 RTC. The external reference can simply be connected to the RTC_I pin. Take care that the 32.768 kHz reference signal is always on and the input voltage is within the RTC_I specification. Adjusting the level can be achieved with a voltage divider. Also make sure the frequency versus temperature behavior of the external clock is within the recommended crystal specification in section 3.3.

☞ Make sure the voltage levels are within datasheet values; see UBX-G7020-Kx Data Sheet [1] or UBX-G7020-CT Data Sheet [2].

2.5.4 Time aiding

Time can also be sent by UBX message at every startup of the UBX-G7020. This can be done to enable warmstart, AssistNow Autonomous and AssistNow Offline. This can be done when no RTC is maintained.

To enable Hotstarts correctly, the time information must be known accurately and thus the TimeMark feature has to be used.

For more information about time aiding or TimeMark see the u-blox 7 Receiver Description including Protocol Specification [3].

☞ For Power Save Mode operations where the RTC is needed the time aiding cannot be used. Because the host does not have any information when the UBX-G7020 turns from OFF status to ON status during ON/OFF operation of Power Save Mode.

2.6 RF front-end

The UBX-G7020 makes use of a RF subsystem, which can receive GPS and GLONASS frequencies. However, because of differing center frequencies the receiver has to be switched to GPS or GLONASS mode by using a UBX message. Parallel reception of both GPS and GLONAS is not possible with the UBX-G7020.

Note that the internal LNA input requires additional matching components to be added depending on the application. The choice of these components affects the RF noise figure and the immunity to out-of-band interference - a major threat for every GPS/GNSS receiver. As both GPS and GLONASS operate with very small received signal levels ranging from -120dBm to about -160dBm any out-band interferer e.g. from GSM, CDMA, WCDMA, WiFi or Bluetooth wireless systems is tens of dB larger. If coupled into the RF front-end the wanted GNSS signal strength will be greatly suppressed reducing the systems sensitivity. The impact is even worse for a larger interferer adjacent to the GNSS frequency bands which may saturate the RF front-end, blocking the GNSS signal. To suppress out-of-band interferers a SAW filters must be added to the design.

Another consequence of the weak GNSS signals is that for best performance the RF noise figure should be as low as possible. Thus an active antenna with integral LNA can be used, or for operation with a passive antenna an external LNA may be used in front of the GNSS chip.

The proper selection and combination of SAW filters and LNA is crucial, because filter losses can increase the RF noise figure and the out-of-band gain of the LNA decreases the jamming immunity. In addition, the bandwidth of the external components including antenna should match the GPS and/or GLONASS signal bandwidth. It should be noted that a GNSS receiver, which is intended to operate with GPS and GLONASS signals must use external RF parts designed to accept both frequency spectra. However, in a GPS only application the external components can have a narrower bandwidth centered at 1575.42MHz. A GLONASS only application would require external components centered at 1602MHz and a bandwidth of about 10MHz. So it might be a challenge, especially for the antenna, to get good performance on GPS and GLONASS signals with the same receiver.

2.6.1 General notes on interference issues

Received GPS/GNSS signal power at the antenna is very low. At the nominal received signal strength (-130dBm) it is ~15 dB below thermal noise. Due to this fact, a GPS/GNSS receiver is susceptible to interference from nearby RF sources of any kind. Two cases can be distinguished:

1. **Out-of-band interference:** Typically any kind of wireless communications system (e.g. GSM, CDMA, 3G, WLAN, Bluetooth, etc.) may emit its specified maximum transmit power in close proximity to the GPS/GNSS receiving antenna, especially if such a system is integrated with the GPS/GNSS receiver. Even at reasonable antenna selectivity, destructive power levels may reach the RF input of the GPS/GNSS receiver. Also, larger signal interferers may generate intermodulation products inside the GPS/GNSS receiver front-end that fall into the GPS/GNSS band and contribute to in-band interference.
2. **In-band interference:** Although the GPS/GNSS band is kept free from intentional RF signal sources by radio-communications standards, many devices emit RF power into the GPS/GNSS band at levels much higher than the GPS/GNSS signal itself. One reason is that the frequency band above 1 GHz is not well regulated with regards to EMI, and even if permitted, signal levels are much higher than GPS/GNSS signal power. Notably, all kind of digital equipment, like PCs, digital cameras, LCD screens, etc. tend to emit a broad frequency spectrum up to several GHz of frequency. Also wireless transmitters may generate spurious emissions that fall into GPS/GNSS band.

As an example, GSM uses power levels of up to 2W (+33 dBm). The absolute maximum power input at the RF input of the GPS/GNSS receiver can be +15dBm. The GSM specification allows spurious emissions for GSM transmitters of up to -36 dBm, while the GPS/GNSS signal is less than -120 dBm. By simply comparing these numbers it is obvious that interference issues must be seriously considered in any design of a GPS/GNSS receiver.

☞ The Inmarsat satellite comms uplink frequency falls adjacent to the GLONASS band. Therefore it is not recommended to integrate a GPS/GLONASS receiver and an Inmarsat terminal within the same design.

Different design goals may be achieved through different implementations:

1. The primary focus is prevention of destruction of the receiver from large input signals. Here the GPS/GNSS performance under interference conditions is not important and suppression of the GPS/GNSS signal is permitted. It is sufficient to just observe the maximum RF power ratings of all the components in the RF input path.
2. GPS/GNSS performance must be guaranteed even under interference conditions. In that case, not only the maximum power ratings of the components in the receive patch must be observed. Further, non-linear effects like gain compression, NF degradation (desensitization) and intermodulation must be analyzed.

☞ Pulsed interference with a low duty cycle like e.g. GSM usually does not affect GPS/GNSS performance but may be destructive due to the high peak power levels.

2.6.1.1 In-band interference mitigation

With in-band interference the signal frequency is very close to the GPS/GNSS frequency of 1575 MHz (see Figure 14). Such interference signals are typically caused by harmonics from displays, micro-controller operation, bus systems, etc.

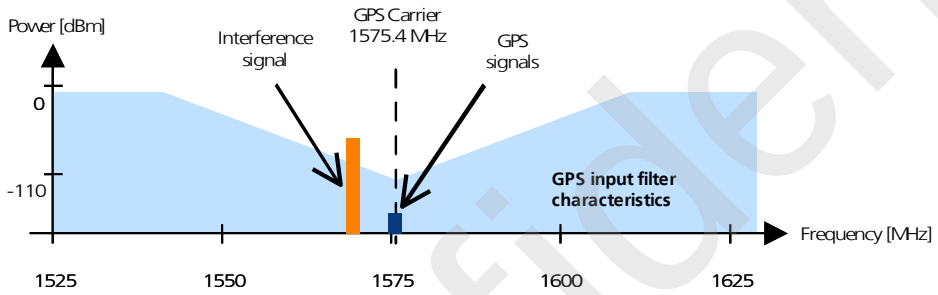


Figure 14: In-band interference signals

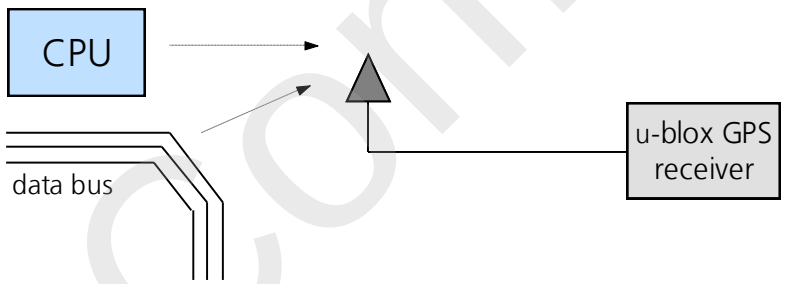


Figure 15: In-band interference sources

Measures against in-band interference include:

- Maintaining a good grounding concept in the design
- Shielding
- Layout optimisation
- Low-pass filtering of noise sources, e.g. digital signal lines
- Remote placement of the GPS/GNSS antenna, far away from noise sources
- Adding a CDMA, GSM, WCDMA,BT band-pass filter before antenna

2.6.1.2 Out-of-band interference

Out-of-band interference is caused by signal frequencies that are different from the GPS/GNSS carrier (see Figure 16). The main sources are wireless communication systems such as GSM, CDMA, WCDMA, WiFi, BT, etc.

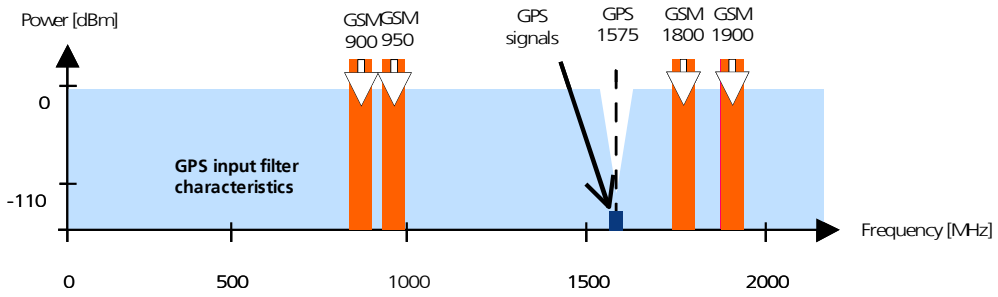


Figure 16: Out-band interference signals

Measures against out-of-band interference include maintaining a good grounding concept in the design and adding a GPS/GNSS band-pass filter into the antenna input line to the receiver.

For GSM applications like a typical handset design an isolation of approximately 20 dB can be reached with careful placement of the antennas. If this is insufficient, an additional input filter is required on the GPS/GNSS receiver input to block the remaining GSM transmitter energy.

2.6.2 RF front-end circuit options

The first stages of the signal processing chain are crucial to the overall receiver performance. Also, in many applications an input connector may be used to receive the RF-input. This can provide a conduction path for harmful or even destructive electrical signals and hence the RF input needs to be protected accordingly.

The following points should be considered seriously in order to determine the appropriate RF-input circuitry:

1. Is the design used to receive GPS only or is it intended to design a combined GPS/GLONASS receiver?
    a. In the latter case special attention has to be taken to the RF band-pass filter (F1). Because GLONASS is received at 1602 MHz instead of 1575.42 MHz for GPS, the filter bandwidth has to be increased (see recommended parts in section 3.5).
    b. If an additional LNA protection filter (F2) shall be used its bandwidth has also to be increased (see recommended parts in section 3.6).
2. What is the expected quality of the signal source (antenna)?
    a. If an external active antenna is to be used, what signal power will be delivered?
    b. If a passive antenna is being used, how susceptible is it to load matching? What is the antenna gain & directivity?
3. Are destructive RF power levels expected to reach the RF-input? Check against the maximum ratings provided in the UBX-G7020-Kx Data Sheet [1] and UBX-G7020-CT Data Sheet [2]!
4. Is interference from wireless transmitters expected?
    a. What are the characteristics of these signals (duty cycle, frequency range, power range, spectral purity)?
    b. What is the expected GPS/GNSS performance under interference conditions?
5. Is there a risk of RF-input exposure to excessive ESD stress?
    a. PCB / system assembly: Is there risk that statically charged parts (e.g. patch antennas) may be discharged through the RF-input?

b. In the field: Is the antenna connector accessible by the user?

The following subsections provide several options addressing the various questions above.

☞ In some applications, such as GSM transceivers, interference signals may exceed the maximum power rating of the LNA_IN input. To avoid device destruction use of external input protection is mandatory.

☞ During assembly of end-user devices which contain passive patch antennas, an ESD discharge may occur during production when pre-charged antennas are soldered to the GPS/GNSS receiver board. In such cases, use of external protection in front of LNA_IN is mandatory to avoid device destruction.

2.6.2.1 RF front-end using a passive antenna

If a passive antenna with high RHCP antenna gain and good sky view is used together with a short 50 ohm line between antenna and receiver, the circuit in Figure 17 can be used. This provides the minimum BoM cost and minimum board space.

Components L1 and C2 serve as input matching for the LNA input. Depending on board layout the values may need to be adjusted to provide a 50 Ohm input impedance. Starting values are provided in sections 3.14 and 3.16, C1 is a DC block.

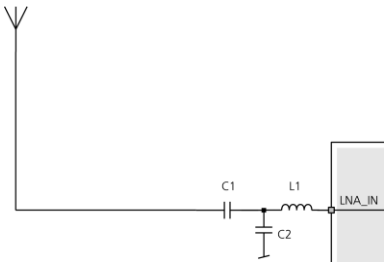


Figure 17: LNA input matching

☞ ESD discharge into the RF input cannot always be avoided during assembly and / or field use with this Circuit! To provide additional robustness an ESD protection diode, as listed in section 3.10, can be placed at LNA_IN to GND.

☞ There is no internal DC blocking capacitor at the LNA_IN pin. Thus when using a passive antenna with an integral short to GND, e.g. PIF antenna, a DC blocking capacitor C1 between the antenna and matching network is required.

2.6.2.2 External LNA for improved performance

As mentioned earlier an external LNA (U1) will improve the RF noise figure (see Figure 18 below), which results in a better GPS/GNSS performance. Because the out-of-band gain of the external LNA (U1) will increase the sensitivity to interference it is advisable to put an additional SAW filter (F1) between the external LNA (U1) and the UBX-G7020 input matching network.

Components L1 and C2 serve as input matching for the LNA input. Depending on the board layout the values need to be tuned until a 50 Ohm input impedance is achieved. Starting values are provided in Sections 3.14 and 3.16, C1 is a DC block.

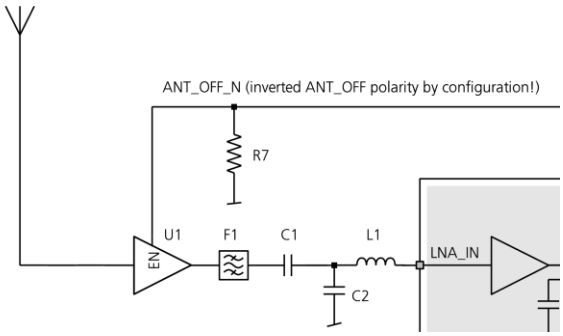


Figure 18: RF path for best GPS/GNSS performance

The LNA (U1) can be selected to deliver the performance needed by the application in terms of:

- Noise figure (sensitivity)
- Selectivity and linearity (Robustness against jamming)
- Robustness against RF power and ESD

☞ The external LNA (U1) must be placed close to the antenna to get best performance.

The PIO16 (ANT_OFF_N) signal can be used to enable and disable the external LNA to lower power consumption, e.g. in Power Save Mode. To enable this, PIO16 must be configured via the Low Level Configuration to provide the ANT_OFF function with the correct polarity - ANT_OFF_N signal. This configuration is part of the antenna supervisor section within the Low Level Configuration, see section 2.10.2.

☞ A pull-down resistor (R7) is required to ensure correct operation of the ANT_OFF_N signal at PIO16.

2.6.2.3 Improved jamming immunity

If the UBX-G7020 is exposed to an interference environment it is recommended to use additional filtering. Improved interference immunity with good GPS/GNSS performance is achieved when using a SAW/LNA/SAW configuration between the antenna and the UBX-G7020 matching network. The single-ended SAW Filter F2 (see section 3.6) can be placed in front of the LNA matching network to prevent saturation caused by very strong interferers.

Components L1 and C2 serve as input matching for the LNA input. Depending on the board layout the values need to be tuned until a 50 Ohm input impedance is achieved. Starting values are provided in Sections 3.14 and 3.16, C1 is a DC block.

It should be noted that the insertion loss of filter F2 directly affects the system noise figure and hence the system performance. Choice of a component with low insertion loss is mandatory when a passive antenna is used with this set-up.

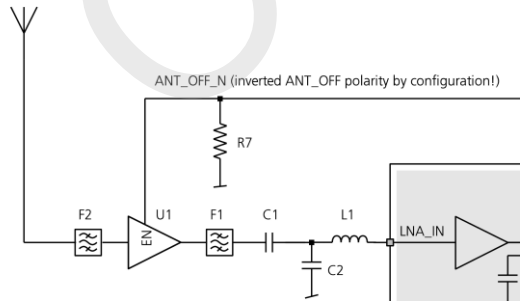


Figure 19: Jamming Immune RF input with good GPS/GNSS performance

ESD discharge can't be avoided during assembly and / or field use. Note also that SAW filters are susceptible to ESD damage.

The PIO16 (ANT_OFF_N) can be used to enable and disable the external LNA for improved power savings, e.g. in Power Save Mode. To enable this, PIO16 must be configured via the Low Level Configuration to provide the ANT_OFF function with the correct polarity - ANT_OFF_N signal. This configuration is part of the antenna supervisor section within the Low Level Configuration, see section 2.10.2.

☞ A pull-down resistor (R7) is required to ensure correct operation of the ANT_OFF_N signal at PIO16.

2.6.2.4 RF front-end using an active antenna

Active antennas for GPS/GNSS application are usually powered through a DC bias on the RF cable. A simple bias-T as shown in Figure 20 can be used to add this DC current to the RF signal line.

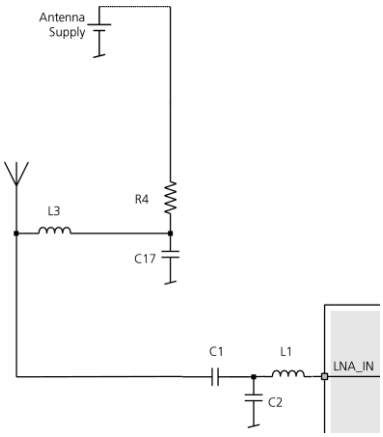


Figure 20: Active Antenna Supply circuit (Bias-T)

L3 isolates RF from the DC path and C17 removes high frequency noise from the DC supply. R4 serves as a current limiter and should be dimensioned to dissipate the power generated by a short on the antenna input. Also, L3 should be selected to pass the DC fault current.

☞ The UBX-G7020 supports antenna supervision by adding external circuitry. For more information please see section 2.2.7.

☞ Make sure the DC block (C1) is in place; the UBX-G7020 LNA_IN has no internal DC block.

2.7 USB

The UBX-G7020 USB interface supports the full-speed data rate of 12 Mbit/s. It is compatible to USB 2.0 FS standard. The interface requires some external components in order to implement the physical characteristics required by the USB 2.0 specification. Figure 21 shows the interface pins and additional external components. In order to comply with USB specifications, VBUS must be connected through a LDO (U2) to pin VDD_USB of the UBX-G7020. This ensures that the internal 1.5k pull-up resistor on USB_DP gets disconnected when the USB host shuts down VBUS.

Depending on the characteristics of the LDO (U2) it is recommended to add a pull-down resistor (R8) at its output to ensure VDD_USB does not float if a USB cable is not connected, i.e. when VBUS is not present.

The interface can be used either in "self powered" or "bus powered" mode. The required mode can be configured with the Low Level Configuration setting. Also, the default vendor ID, vendor string, product ID and product string can be changed via Low Level Configuration settings and held permanently in external SQI flash or internal eFuse, see section 2.10.2.

In order to get the 90 ohm differential impedance in between the USB_DM and USB_DP data line a 27ohm series resistor (R1,R2) must be placed into each data line (USB_DM and USB_DP).

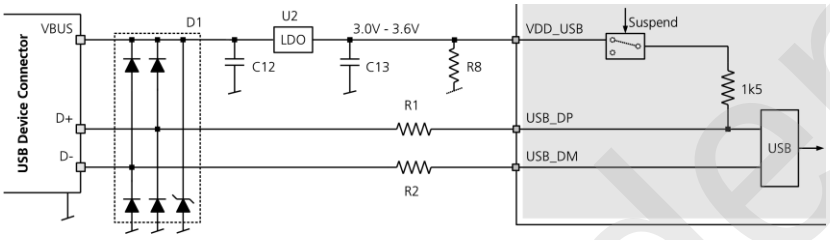


Figure 21: USB interface

Name	Component	Function	Comments
U2	LDO	Regulates VBUS (4.4 …5.25 V) down to a voltage of 3.3 V).	Almost no current requirement (~1 mA) if the GPS receiver is operated as a USB self-powered device, but if bus-powered LDO (U1) must be able to deliver the maximum current of ~100 mA, depending if the DCDC converter option is used.
C12, C13	Capacitors		Required according to the specification of LDO U2
D1	Protection diodes	Protect circuit from overvoltage / ESD when connecting.	Use low capacitance ESD protection such as ST Microelectronics USBLC6-2.
R1, R2	Serial termination resistors	Establish a full-speed driver impedance of 28…44 Ohms	A value of 27 Ohms is recommended.
R8	Resistor	Ensures defined signal at VDD_USB when VBUS is not connected / powered	1k Ohms is recommended for USB self-powered setup. For bus-powered setup R11 is not required.

Table 10: Summary of USB external components

See section A.7 and A.8 for reference schematics for self- and bus-powered operation.

☞ If the USB interface is not used, connect VDD_USB to GND.

2.8 JTAG

A JTAG interface can be used for testing and debugging. This interface allows failure analysis by the factory and boundary scan in production test.

Pin	Function	Remarks
TDI / PIO13	Test Data Input	Shared with PIO13
TDO / PIO14	Test Data Output	Shared with PIO14
TMS	Test Mode Select	
TCK	Test Clock	

Table 11: JTAG interface

2.9 Layout

2.9.1 Placement

GPS signals at the surface of the Earth are about 15dB below the thermal noise floor. A very important factor in achieving maximum GPS/GNSS performance is the placement of the receiver on the PCB. The Placement used may affect RF signal loss from antenna to receiver input and enable interference into the sensitive parts of the receiver chain, including the antenna itself. When defining a GPS receiver layout, the placement of the antenna with respect to the receiver, as well as grounding, shielding and interference from other digital devices are crucial issues and need to be considered very carefully.

Signal loss on the RF connection from antenna to receiver input must be minimized as much as possible. Hence the connection to the antenna must be kept as short as possible. Doing this will help avoiding interference into the very sensitive RF section.

Make sure that RF critical circuits are clearly separated from any other digital circuits on the system board. To achieve this, position the receiver digital part towards your digital section of the system PCB and have the RF section and antenna placed as far as possible away from the other digital circuits on the board.

A proper GND concept shall be followed: The RF section should not be subject to noisy digital supply currents running through its GND plane.

Care must also be exercised with placing the receiver in proximity to circuitry that can emit heat. The RF part of the receiver is very sensitive to temperature and sudden changes can have an adverse impact on performance.

The crystal or TCXO of a GPS receiver is a temperature sensitive device. Avoid high temperature drift and air convection.

Crystal oscillator circuits are very sensitive to noise from adjacent lines. This is especially true for the high-impedance RTC circuit. It is strictly recommended to use an appropriate guard ring design in order to shield the crystal circuit from crosstalk.

2.9.2 Package footprint, copper and solder mask

Copper and solder mask dimensioning recommendations for the UBX-G7020 packages are provided in this section. For all packages, the yellow color shows the copper (etch) dimensions, the green color shows the solder mask opening dimensions and the red circles indicate vias. Some PCB manufacturers prefer to adapt solder mask openings to their process tolerances. The recommendations given in this section provide the nominal openings not including such additional tolerances.

Paste mask recommendations are not provided as these are usually specifically related to the solder paste in use as well as the particular reflow process.

2.9.2.1 QFN40 Package

Note the placement of GND vias inside the center GND plane of the package. As these vias are covered with solder mask, there is no risk of solder paste being sucked into via holes during reflow. The landing pads for the exterior pads extend slightly beyond the maximum package dimensions.

The checkerboard pattern of the solder mask opening ensures even distribution of solder paste across the large center GND pad. Units below are in mm.

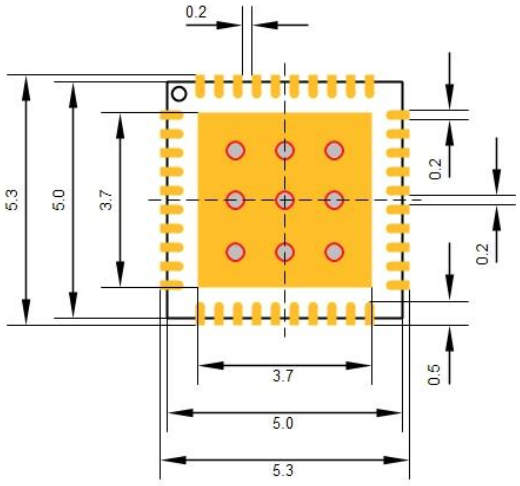


Figure 22: QFN40 (UBX-G7020-Kx) recommended copper land pattern

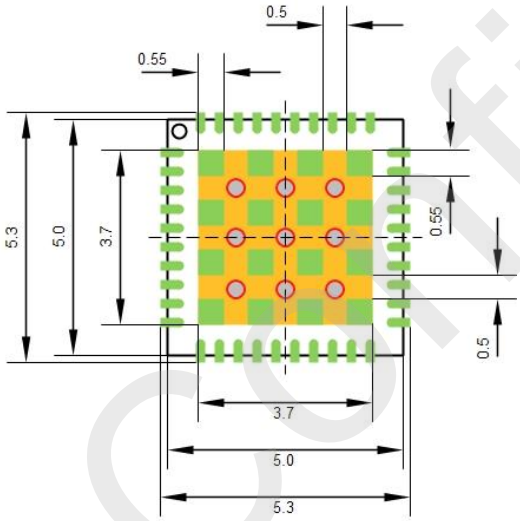


Figure 23: QFN40 (UBX-G7020-Kx) recommended solder mask opening pattern

☞ For mechanical specifications see UBX-G7020-Kx Data Sheet [1].

2.9.2.2 WL-CSP50 Package

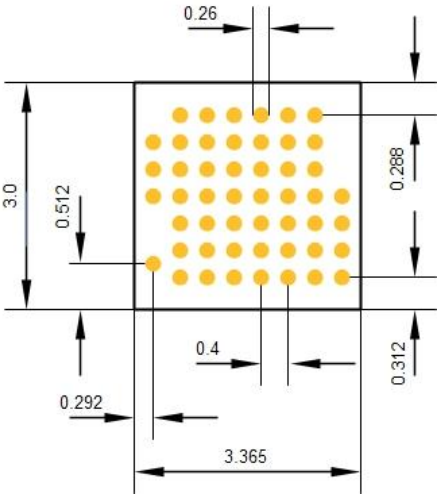


Figure 24: QFN40 (UBX-G7020-CT) recommended copper land pattern

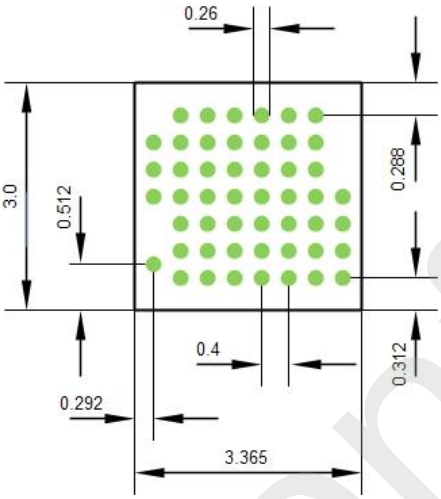


Figure 25: QFN40 (UBX-G7020-CT) recommended solder mask opening pattern

☞ For mechanical specifications see UBX-G7020-CT Data Sheet [2].

2.10 System Configuration

The UBX-G7020 applies the following configurations at startup:

1. Communication Interface Configuration
2. Low Level Configuration
3. Functional Configuration

2.10.1 Communication Interface Configuration

The Communication Interface Configuration selects the interface for communication to the host CPU. The selection is done according to the status of PIO10 (D_SEL pin). See section 2.2.3, Table 5.

2.10.2 Low Level Configuration

The low level configuration defines all the important system related settings and needs to be set initially in production. It is mandatory for the UBX-G7020 that the Low Level Configuration is set correctly, otherwise it will not work properly or may even not start up at all.

All the Low Level Configurations can be set in the eFuse inside the UBX-G7020 chip. If an SQI Flash is connected to the UBX-G7020 a partial Low Level Configuration, i.e. all except the VDD_IO POR threshold can be saved permanently in the SQI Flash. If no SQI Flash is connected some of the Low Level Configuration can be set by configuration pins.

The parts of the Low Level Configuration held in the SQI Flash or set by Configuration Pins have higher priority than the Low Level Configuration held within the UBX-G7020 eFuse.

If the clock/oscillator Low Level Configuration settings are incorrect, it is mandatory to start up in the Safe Boot Mode. To do this, PIO12 the SAFEBOOT_N pin, must be low (see section 2.2.6) on startup. Usually this is required with an SQI flash based design starting for the first time in production. That is, the eFuse settings are not configured and the SQI flash has not yet been programmed with information about the clock/oscillator.

Topic	Setting	Description	Default Setting	Remarks
UART	UART Baud Rate	Configures the Baud Rate	9600 baud	
	UART Remapping	In case SPI is used for communication to host, UART can be remapped to PIO15 and PIO16 if needed	Not remapped	Remapped UART cannot be used in Safe Boot Mode!
SQI Flash	VDD_IO POR	Sets the threshold for the VDD_IO POR. The VDD_IO POR threshold needs to be set according to supply voltage range of external SQI Flash (1.8V / 3V).	1.8V	**Must be always configured in eFuse!**
Power	DCDC converter	Enables the optional DCDC converter	Disabled	
Main Clock	Single Crystal	RTC is derived from Main Clock (no RTC crystal needed)	Disabled	
	Clock type	What kind of clock source is used; TCXO or Crystal	Crystal	
	Clock data	Additional information to the clock source; load of crystal or supply of TCXO	19pF load	
Active Antenna / LNA	Antenna supervisor/ external LNA enable pin	There are 2 different antenna supervisors available, a 2-pin and a 3-pin version. Additionally on enable signal can be made available to turn off external LNA in Power Save Mode.	2-pin Antenna Supervisor	ANT_OFF and ANT_OK
	Polarity of Antenna supervisor / LNA enable pin	Polarity of the antenna supervisor pins/ LNA enable pin can be configured.		
USB	USB powered mode	Self or bus powered device	Self powered	
	USB vendor ID	Sets the vendor ID	0x1546	
	USB vendor string	Sets the vendor string	u-blox AG - www.u-blox.com	
	USB product ID	Sets the product ID	0x01A7	
	USB product string	Sets the product string	u-blox 7 - GPS/GNSS Receiver	

Table 12: Low Level Configuration overview and default settings

For detailed information about how to set the Low Level Configuration in SQI flash or eFuse see u-blox 7 Receiver description including protocol specification [3].

☞ The VDD_IO threshold (POR_IO) which has to match the supply voltage of the SQI flash, must be always configured in eFuse; must not be set in SQI Flash!

The current Low Level Configuration can be checked by polling the UBX-MON-LLC message, see u-blox 7 Receiver description including protocol specification [3].

2.10.2.1 One Time Programmable eFuse

The UBX-G7020 eFuse is implemented as an OTP memory which can hold all the Low Level Configuration settings. The eFuse is supplied by VDD_IO and consumes ~10mA during writing.

The eFuse can be accessed and changed by any communication port. To write a Low Level Configuration into the eFuse, the UBX-CFG-OTP message has to be used. For detailed information see u-blox 7 Receiver description including protocol specification [3].

In Safe Boot Mode (e.g. in production for designs with external SQI flash) the eFuse cannot be accessed by USB, because of the unknown main clock source, see section 2.2.6. Access via UART is possible after sending a training sequence to the UBX-G7020. With a remapped UART it is not possible to communicate to the UBX-G7020 in Safe Boot Mode. A DDC and SPI communication method is the most convenient mode to set the eFuse Low Level Configuration correctly as the clock is provided by the host.

☞ VDD_IO monitor level (POR_IO) level must always be set in eFuse!

2.10.2.2 Low Level Configuration by Configuration Pins (for designs without external SQI Flash)

If no external SQI Flash is connected, PIO0 to PIO5 can be used for some low level configuration settings. If PIO5 (CONFIG_SEL), is connected to GND it enables the Low Level Configuration pins PIO0 to PIO4. The part of the Low Level Configuration set by the configuration pins has a higher priority than the Low Level Configuration held in the eFuse. For information about the Low Level Configuration pins see section 2.2.2.

With the Low Level Configuration set by the configuration pins, it should be able to start up with the correct clock/oscillator setting to enable the host to communicate with the UBX-G7020. Thus starting in Safe Boot Mode is not required and the host is able to communicate with the UBX-G7020 to set the eFuse Low Level Configuration.

☞ All UBX-G7020 ROM based designs using the default clock frequency with PIO0 to PIO5 set correctly are able to communicate to a host by UART, DDC, SPI, or USB without entering the Safe Boot Mode.

☞ All UBX-G7020 ROM based designs using the default clock frequency and set the PIO0 to PIO5 correctly, are able to communicate to a host without entering the Safe Boot Mode by UART, DDC, SPI, or USB.

2.10.2.3 Low Level Configuration saved in SQI Flash

If the firmware runs out of SQI flash, partial Low Level Configuration can be saved in the SQI flash too. Thus the Low Level Configuration can be changed more often compared to the one time programming of the eFuse. The part of the Low Level Configuration set in SQI flash has a higher priority than the Low Level Configuration set by the eFuse!

If the SQI flash is only used to log data, the Low Level Configuration cannot be saved in the SQI flash. Only if the firmware runs from the SQI flash can the Low Level Configuration be saved in the SQI flash.

If an SQI flash is connected to the UBX-G7020 without valid firmware contents (e.g. corrupted firmware code or none programmed), it will then only use the Low Level configuration from eFuse. So if the firmware gets corrupted, the receiver might not run at all, because of a potentially wrong Low Level Configuration.

☞ Even if all the Low Level Configuration can be saved in SQI flash it is recommended to also set all the Low Level Configuration in the eFuse as well. Thus if the SQI flash contents becomes corrupted the UBX-G7020 is still able to start up correctly and the flash can be subsequently reprogrammed.

☞ For designs with external SQI Flash and not using default clock settings (26MHz, 19pF crystal) it is mandatory to initially startup in the Safe Boot Mode. Hence there must be a method to pull-down the PIO12 (SAFEBOOT_N pin) during production!

A design using USB and SQI flash, but not using the clock/oscillator default settings must start up in production in Safe Boot Mode. Owing to the internal ring oscillator it cannot use USB and hence will require another communication interface to program the flash in production

2.10.2.4 Low Level Configuration applying sequence

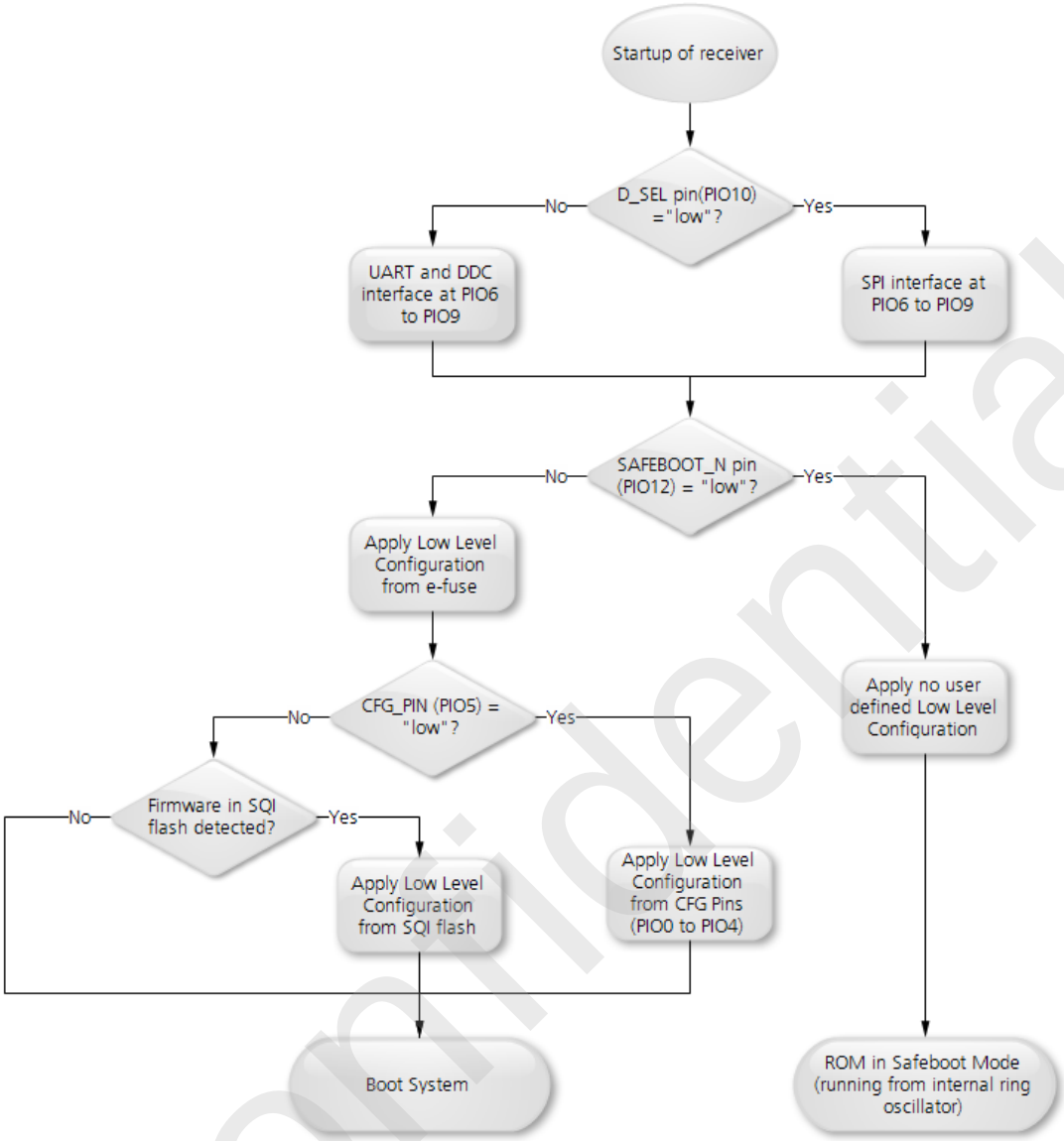


Figure 26: Low level configuration applying sequence

☞ The Low Level Configuration can be checked with the UBX-MON-LLC message.

2.10.3 Functional configuration

After the Low Level Configuration has been applied and provided that the system is not in Safe Boot Mode, the Functional Configuration is applied. The Functional Configuration specifies a wide range of parameters like the configuration of the communication ports, navigation engine settings and message protocol selection. This information can be stored in the backup memory or the SQI flash, if present.

If the Functional Configuration is saved to backup memory without its associated backup battery (i.e. V_BCKP not supplied independently from VDD_IO), then if VDD_IO fails the backup memory (BBR) is not maintained. Hence the current functional configuration will becomes lost and must be sent to the UBX-G7020 on every startup. A Functional configuration stored in SQI flash will remain valid between power cycles.

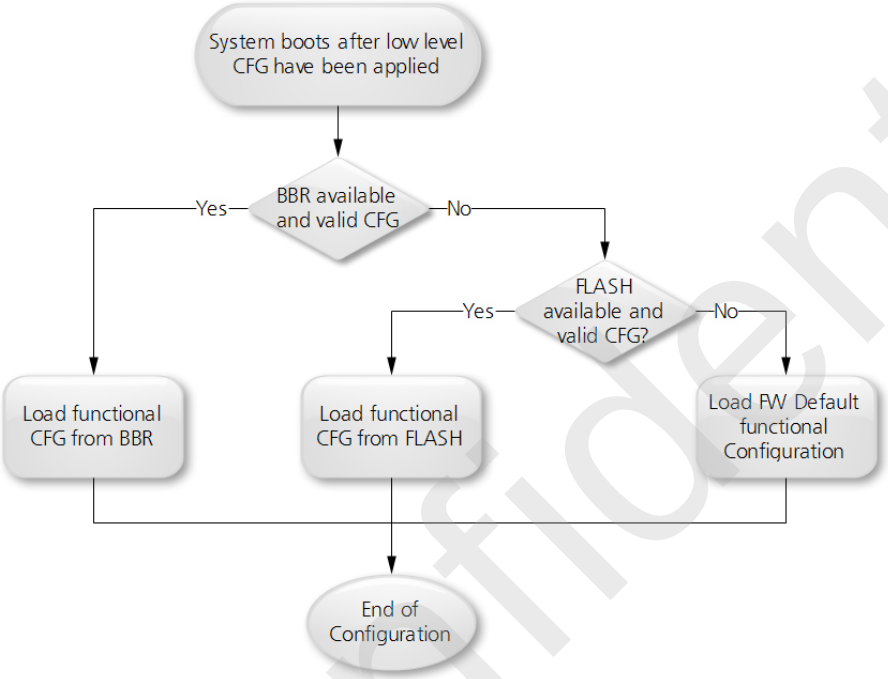


Figure 27: Functional Configuration Sequence

2.10.4 Functional configuration at run time

Of course the Functional Configuration can be sent by the host at run time or can be fed to the UBX-G7020 at every start up, for example in a ROM based design.

3 Component Selection

This section provides some information on components that are critical for the performance of the UBX-G7020 chip. Of course, temperature range specifications need only be as wide as required by a particular application.

3.1 TCXO (Y1)

ID	Parameter	Value
1	**Frequency Specifications**	
1.1	Nominal frequency at 25ºC	26 MHz (other frequencies possible, see datasheet[1])
1.2	Frequency calibration tolerance at 25ºC	< ±2.0 ppm
1.3	Operating temperature range I	-40 °C … +85 °C
1.4	Operating temperature range II	-30 °C … +85 °C
1.5	Frequency stability over operating temperature range I referenced to the midpoint between min. and max. frequency value over this temperature range	< ±2.5 ppm
1.6	Frequency stability over operating temperature range II referenced to the midpoint between min. and max. frequency over this temperature range	< ±0.5 ppm
1.7	Frequency slope[2] over -30ºC to 85ºC	< 0.1 ppm / ºC
1.8	Frequency slope[3] over -40ºC to -30ºC	< 0.5 ppm / ºC
1.9	Static temperature hysteresis[4]	< ±0.6 ppm
1.10	Supply Voltage Stability, ±5% supply voltage change at 25ºC	< ±0.1 ppm
1.11	Load Sensitivity, ±10% load change at 25ºC	< ±0.2 ppm
1.12	Long term stability, frequency drift over 1 year	< ±1.0 ppm
1.13	Long term stability, frequency drift over 2 years	< ±2.0 ppm
1.14	Long term stability, frequency drift over 10 years	< ±4.0 ppm
1.15	G Sensitivity, all 3 axes, random vibration, 30 Hz to 1.5 kHz	< 1.5E-9 (1.5 ppb) per G
1.16	Shock, frequency shift after 1000G 250 µs sine	< ±0.5 ppm
2	**Electrical Specifications**	
2.1	Supply Voltage[5]	1.75 – 2.0 V or 2.5 – 3.6 V
2.2	Supply Current at maximum supply voltage	< 1.5 mA
3	Oscillator output	
3.1	Output Waveform	DC coupled clipped sine wave
3.2	Output voltage level peak to peak at minimum supply voltage	> 0.8 V
3.3	Output voltage DC offset	
3.4	Output load resistance	9.0 – 11.0 kΩ
3.5	Output load capacitance	9.0 – 11.0 pF
4	**SSB phase noise**	
4.1	Typical SSB Phase Noise Density, 1 Hz offset	< -57 dBc/Hz
4.2	Typical SSB Phase Noise Density, 10 Hz offset	< -88 dBc/Hz
4.3	Typical SSB Phase Noise Density, 100 Hz offset	< -112 dBc/Hz
4.4	Typical SSB Phase Noise Density, 1 kHz offset	< -130 dBc/Hz
4.5	Typical SSB Phase Noise Density, 10 kHz offset	< -140 dBc/Hz
5	**Environmental specifications**	
5.1	Shock	Half sine wave acceleration of 100 G peak amplitude for 11 ms

[1] UBX-G7020-Kx Data Sheet [1] and UBX-G7020-CT Data Sheet [2].
[2] Minimum of 1 frequency reading every 2ºC.
[3] Minimum of 1 frequency reading every 2ºC.
[4] Frequency change after reciprocal temperature ramped over the operating temperature range I. Frequency measured before and after at 25ºC.
[5] Depends on system supply voltage, see section 2.4.5.

ID	Parameter	Value
		duration, 3 cycles each plane
5.2	Vibration	10 G RMS 30 Hz to 1500 Hz, duration of 6 hours
5.3	Humidity	48 hours at 85 °C 85% relative humidity non-condensing
5.4	Thermal shock	Exposed at –40 °C for 30 minutes then to 85 °C for 30 minutes constantly for 120 cycles (5 days)
5.5	Storage temperature	-40 °C … +85 °C
6	**Manufacturing information**	
6.1	Solder Process	Able to withstand solder reflow process, min. 3 Cycles (240 °C, 20 s)
6.2	Packaging description	Tape and Reel

Table 13: TCXO specifications

Manufacturer	Order No.	Comments
Rakon	IT2205BE 26.000MHz TX5738	3.0 V TCXO
Rakon	IT5305BE 26.000MHz TX5477	3.0 V TCXO
Rakon	IT2205ME 26.000MHz TX5596	1.75V to 2.0V TCXO

Table 14: Recommended parts list for TCXO

☞ Other TCXOs can be used provided they meet the specifications listed in Table 13. For reliable GPS performance particular attention must be paid to the temperature range and frequency slope specifications.

3.2 Crystal (Y2)

ID	Parameter	Value
1	**Frequency Specifications**	
1.1	Oscillation mode	Parallel Resonance, Fundamental Mode
1.2	Nominal frequency at 25 ± 3 °C[6]	26 MHz (other frequencies possible, see datasheet[7])
1.3	Frequency calibration tolerance at 25 ± 3 °C[8]	< ±7.0 ppm
1.4	Frequency stability over operating temperature range referenced to frequency reading 25 ± 3 °C[9]	< ±15.0 ppm
1.5	Operating temperature range	-40 °C … +85 °C
1.6	Frequency perturbations[10]	< 0.5 ppm
1.7	Static temperature hysteresis[11]	< ±0.4 ppm
1.8	Short term stability, root Allan variance (τ = 1 s)	< 1.0E-9 (1.0 ppb)
1.9	Long term stability, frequency drift over 1 year	< ±1.0 ppm
1.10	Long term stability, frequency drift over 2 years	< ±1.5 ppm
1.11	Long term stability, frequency drift over 10 years	< ±5.0 ppm
1.12	G Sensitivity, all 3 axes, random vibration, 30 Hz to 1.5 kHz	< 1.5E-9 (1.5 ppb) per G
1.13	Shock, frequency shift after 1000G 250 µs sine	< ±0.5 ppm
2	**Electrical Specifications**	
2.1	Load capacitance C_L	19 pF
2.2	Equivalent circuit (shunt) capacitance C_0	< 6 pF
2.3	Pullability	< 12 ppm/pF
2.4	Maximum Drive Level (only at oscillator start-up, if required)	200 µW
2.5	Operating Drive Level	10 - 80 µW, corresponding to 10 – 50 mV
2.6	Drive level dependency (DLD)[12]	< 0.6 Ω
2.7	Equivalent series resistance (ESR)	15 - 60 Ω
3	**Electrical Specifications**	
3.1	Shock	Half sine wave acceleration of 100 G peak amplitude for 11 ms duration, 3 cycles each plane
3.2	Vibration	10 G RMS 30 Hz to 1500 Hz, duration of 6 hours
3.3	Humidity	48 hours at 85 °C 85% relative humidity non-condensing
3.4	Thermal shock	Exposed at –40 °C for 30 minutes then to 85 °C for 30 minutes constantly for 120 cycles (5 days)
3.5	Storage temperature	-40 °C … +85 °C
4	**Manufacturing Information**	
4.1	Solder Process	Able to withstand solder reflow process, min. 3 Cycles (240 °C, 20 s)
4.2	Packaging description	Tape and Reel

Table 15: GPS crystal specifications

Manufacturer	Order No.
Rakon	IEC19RSX-8 26.000MHz XZC918
Rakon	IEC19RSX−10 26.000 MHz XZD182

Table 16: Recommend parts list for GPS reference crystal

[6] A reference temperature can be defined with crystal supplier within this range.
[7] UBX-G7020-Kx Data Sheet [1] and UBX-G7020-CT Data Sheet [2].
[8] Same reference temperature as in 2.2
[9] Same reference temperature as in 2.2
[10] Peak to peak deviation from the frequency versus AT temperature curve fit. Minimum of 1 frequency reading every 3 °C over operating temperature range. 100% testing and screening for frequency perturbations and micro jump occurrence.
[11] Frequency change after reciprocal temperature ramped over the operating temperature range. Frequency measured before and after at 25 °C.
[12] Resistance change of 10 different power levels from 0.001 µW to 100 µW

☞ Other crystals can be used provided they meet the specifications listed in Table 15. For reliable GPS performance particular attention must be paid to the temperature range and frequency slope specifications.

3.3 RTC crystal (Y3)

ID	Parameter	Value
1	**Frequency Specifications**	
1.1	Oscillation mode	Fundamental Mode
1.2	Nominal frequency at 25 °C	32.768 kHz
1.3	Frequency calibration tolerance at 25 °C	< ±100 ppm
2	**Electrical specifications**	
2.1	Load capacitance C_L	7 pF
2.2	Equivalent series resistance R_S	< 100 kΩ

Table 17: RTC crystal specifications

Manufacturer	Order No.
Micro Crystal	CC7V-T1A 32.768 kHz 7.0 pF +/- 100 ppm

Table 18: Recommend parts list for RTC crystal

3.4 SQI flash (U3)

Manufacturer	Order No.	Comments
SST	SST26VF016	3V, 16Mb, several package/temperature options
SST	SST26VF032	3V, 32Mb, several package/temperature options
Spansion	S25FL004K	3V, 4Mb, several package/temperature options
Spansion	S25FL008K	3V, 8Mb, several package/temperature options
Spansion	S25FL016K	3V, 16Mb, several package/temperature options
GigaDevice	GD25Q40	3V, 4Mb, several package/temperature options
Macronix	MX25L8035E	3V, 8Mb, **cannot be used for data logging**

Table 19: Recommend parts list for SQI flash

3.5 RF band-pass filter (F1)

Depending on the application circuit, consult manufacturer datasheet for DC, ESD and RF power ratings!

Manufacturer	Order No.	System supported	Comments
TDK/ EPCOS	B8401: B39162-B8401-P810	GPS+GLONASS	High attenuation
TDK/ EPCOS	B3913: B39162B3913U410	GPS+GLONASS	For automotive application
muRata	SAFEA1G58KA0F00	GPS+GLONASS	Only for mobile application
muRata	SAFFB1G58KA0F0A	GPS+GLONASS	Only for mobile application
Triquint	856561	GPS	Compliant to the AEC-Q200 standard

Table 20: Recommend parts list for RF band-pass filter

3.6 External LNA protection filter (F2)

Manufacturer	Order No.	System supported	Comments
TDK/ EPCOS	B8401: B39162-B8401-P810	GPS+GLONASS	High attenuation
TDK/ EPCOS	B3913: B39162B3913U410	GPS+GLONASS	For automotive application
TDK/ EPCOS	B9850: B39162B9850P810	GPS	Low insertion loss
TDK/ EPCOS	B8400: B39162B8400P810	GPS	ESD protected and high input power
muRata	SAFEA1G58KB0F00	GPS+GLONASS	Low insertion loss, only for mobile application
muRata	SAFEA1G58KA0F00	GPS+GLONASS	High attenuation, only for mobile application
muRata	SAFFB1G58KA0F0A	GPS+GLONASS	High attenuation, only for mobile application
muRata	SAFFB1G58KB0F0A	GPS+GLONASS	Low insertion loss, Only for mobile application
Triquint	B9850	GPS	Compliant to the AEC-Q200 standard
CTS	CER0032A	GPS	Ceramic filter also offers robust ESD Protection

Table 21: Recommended parts for the LNA protection filter

3.7 USB line protection (D1)

Manufacturer	Order No.
ST Microelectronics	USBLC6-2

Table 22: Recommend parts list for USB line protection

3.8 USB LDO (U3)

Manufacturer	Order No.
Seiko Instruments Inc.	S-1206B33-I6T2G

Table 23: Recommend parts list for USB LDO

3.9 External LNA (U1)

ID	Parameter	Value
1	**Gain and Noise Figure @ 1.575 GHz**	
1.1	Gain	> 17 dB
1.2	Noise Figure	< 2 dB

Table 24: External LNA specifications

Manufacturer	Order No.	Comments
Maxim	MAX2659ELT+	Low noise figure, up to 10 dBm RF input power
JRC New Japan Radio	NJG1143UA2	Low noise figure, up to 15 dBm RF input power
Avago	ALM-1912	Module, for GPS only, also including FBAR filter in front of LNA
Avago	MGA-231T6	Up to 13 dBm RF input power
Avago	ALM-2712	Module, for GPS only, FBAR filter-LNA filter FBAR

Table 25: Recommend parts list for external LNA

3.10 LNA_IN ESD protection diode (D1)

Manufacturer	Order No.
ON Semiconductor	ESD9R3.3ST5G

Table 26: Recommend parts list for LNA_IN ESD protection diode

3.11 Operational amplifier (U6)

Manufacturer	Order No.
Linear Technology	LT6000
Linear Technology	LT6003

Table 27: Recommend parts list for Operational Amplifier

3.12 Open-drain buffer (U4, U7 and U8)

Manufacturer	Order No.
Fairchild	NC7WZ07P6X

Table 28: Recommend parts list for open-drain buffer

3.13 Antenna supervisor switch transistor (T1)

Manufacturer	Order No.
Vishay	Si1016X-T1-E3

Table 29: Recommend parts list for antenna supervisor switch transistor (p-channel MOSFET)

3.14 RF inductors

Name	Use	Figure	Type / Value
L1	RF-input matching network	Figure 17	8.2N 2%
L3	RF Bias-T	Figure 20	27N 5% (Impedance > 500 ohm @GPS frequency)

Table 30: RF inductors

Manufacturer	Order No.
Murata Manufacturing Company, Ltd.	LQG15H Series
Murata Manufacturing Company, Ltd.	LQP15M Series
Murata Manufacturing Company, Ltd.	LQW15A Series

Table 31: Recommend parts list for RF inductors

☞ The inductance of an inductor also depends on the signal frequency. When selecting a particular inductor the inductance value at 1.575 GHz must match the value provided in Table 30.

3.15 Inductor for DCDC converter (L2)

ID	Parameter	Value
1.1	Self resonance frequency (SRF)	> 30 MHz
1.2	DC resistance (DCR)	< 0.2 Ohm
1.3	Rated current	> 0.5 A
1.3	Inductance	1.0…2.2 uH

Table 32: DCDC inductor specifications

☞ It is recommended to use a shielded inductor.

Manufacturer	Order No.	Comments
muRata	LQM2MPN2R2NG0	Low DCR, for best efficiency of DCDC (~85%)
muRata	LQM21PN1R0MC0	Low height, 0.5mm

Table 33: Recommend parts list for DCDC inductor

3.16 Standard capacitors

Name	Use	Figure	Type / Value
C1	RF-input DC block	Figure 17	COG 47P 5% 25V
C2	RF-input matching network	Figure 17	COG 2P7 +/-0.1P 50V
C3	Decoupling VDD_LNA / VDD_ANA	Figure 5	X5R 1U0 10% 6.3V
C4	Decoupling LDO_RF_OUT	Figure 2	X5R 1U0 10% 6.3V
C5	Decoupling LDO_X_OUT	Figure 2	X5R 1U0 10% 6.3V
C6	Decoupling V_CORE (DCDC converter used)	Figure 3	X5R 4U7 10% 6.3V
C7	Decoupling V_DCDC_IN	Figure 3	X5R 4U7 10% 6.3V
C8	Decoupling VDD_IO	Figure 2	X5R 1U0 10% 6.3V
C9	Decoupling V_BCKP	Figure 2	X5R 1U0 10% 6.3V
C10	Decoupling LDO_B_OUT	Figure 2	X5R 2U2 10% 6.3V
C11	Decoupling V_CORE	Figure 2	X5R 1U0 10% 6.3V
C12	Decoupling of USB LDO	Figure 21	Depends on USB LDO (U2) specification
C13	Decoupling of USB LDO	Figure 21	Depends on USB LDO (U2) specification
C14	Load capacitor at XTAL_O	Figure 9	COG 33P 1% 25V
C15	Load capacitor at XTAL_I	Figure 9	COG 27P 1% 25V
C16	Decoupling LDO_C_OUT	Figure 2	X5R 1U0 10% 6.3V
C17	Bias-T	Figure 20	X7R 10N 10% 16V
C18	Decoupling VDD_IO at SQI flash supply pin	Figure 2	X5R 1U0 10% 6.3V

Table 34: Standard capacitors

3.17 Standard resistors

Name	Use	Figure	Type / Value
R1	USB data serial termination	Figure 21	27R 5% 0.1W
R2	USB data serial termination	Figure 21	27R 5% 0.1W
R8	Pull-down at VDD_USB	Figure 21	1K 5% 0.1W
R3	Pull-up at antenna supervisor transistor	Figure 7 Figure 8	100K 5% 0.1W
R4	Antenna supervisor current limiter	Figure 7 Figure 8	10R 5% 0.25W
R5	Antenna supervisor voltage divider	Figure 8	560R 5% 0.1W
R6	Antenna supervisor voltage divider	Figure 8	100K 5% 0.1W
R7	Pull-down at LNA enable	Figure 18	10K 5% 0.1W

Table 35: Standard resistors

3.18 Ferrite beads (FB1)

Manufacturer	Order No.	Comments
MuRata	BLM15HD102SN1	High impedance @ 1.575 GHz
MuRata	BLM15HD182SN1	High impedance @ 1.575 GHz

Table 36: Recommend parts list for ferrite beads FB1

3.19 Feed-thru capacitors

Manufacturer	Order No.	Comments
MuRata	NFL18SP157X1A3	For data signals, 34 pF load capacitance
MuRata	NFA18SL307V1A45	For data signals, 4 circuits in 1 package
MuRata	NFM18PC474R0J3	For power supply < 2 A, size 0603
MuRata	NFM21PC474R1C3	For power supply < 4 A, size 0805

Table 37: Recommend parts list for feed thru capacitors

4 Design-in Checklists

This section summarizes the most important items for a simple design check. The Layout Design-In Checklist also helps to avoid an unnecessary re-spin of the PCB and helps to achieve the best possible performance. Basically the checklist lists the recommendation from the previous sections.

☞ It is highly recommended to follow the Design-In Checklist when developing any u-blox 7 GPS/GNSS applications. This can significantly reduce development time and costs.

4.1 Pin list

Pin No MLF40 (WL-CSP50)	Name	I/O	Description	Remarks
1 (E2)	VDD_ANA	I	Supply for analog part	Has to be supplied by LDO_RF_OUT, pin 38 (F3). It is recommended to add some filtering, see Figure 5.
2 (E3)	LDO_X_OUT	O	Clock domain voltage	1.0uF to GND. Supply and/ or enable for TCXO
3 (H4)	XTAL_I	I	Main oscillator input	No DC block needed.
4 (H5)	XTAL_O	O	Main oscillator output	Leave open in case TCXO used.
5 (C1)	LDO_B_OUT	O	Backup domain voltage	2.2uF to GND.
6 (C2)	V_BCKP	I	Backup Supply	1.0uF to GND. Connect to VDD_IO if not used.
7 (B1)	VDD_IO	I	PIO and backup supply	1.0uF capacitor to GND.
8 (C3)	USB_DM	I/O	USB data	27 ohm external series resistor. Leave open if not used.
9 (B2)	VDD_USB	I	USB interface supply	Connect to GND if not used.
10 (B3)	USB_DP	I/O	USB data	27 ohm external series resistor. Leave open if not used.
11 (A3)	RTC_O	O	RTC oscillator output	Leave open if not used.
12 (A2)	RTC_I	I	RTC oscillator input	Connect to GND if not used.
13 (B4)	PIO14	I		Leave open if not used.
14 (C4)	PIO13	I		Leave open if not used.
15 (A4)	TCK		JTAG interface	Leave open if not used.
16 (C5)	TMS		JTAG interface	Leave open if not used.
17 (B5)	RESET_N	I	Reset input	Leave open if not used.
18 (A6)	PIO7	I	UART RX/ SPI MOSI	UART RX or SPI MOSI, leave open if not used.
19 (A5)	PIO6	O	UART TX/ SPI MISO	UART TX or SPI MISO, leave open if not used.
20 (C6)	T_SENSE	I/O	Temperature sensing	Leave open.
21 (A7)	V_DCDC_IN	I	DCDC converter input	Connect to V_DCDC_O and V_CORE if not used.
22 (B6)	V_DCDC_OUT	O	DCDC converter output	Connect to V_DCDC_I and V_CORE if not used.
23 (C7)	V_CORE	I	Supply for core and RF domain	Connect to main supply or to DCDC converter inductor.
24 (D7)	LDO_C_OUT	O	Core domain voltage	1.0uF capacitor to GND.
25 (D8)	PIO0	O/I	SQI flash data 0 or config pin	
26 (F8)	PIO4	O/I	SQI flash clock or config pin	
27 (E8)	PIO2	O/I	SQI flash data 2 or config pin	
28 (E7)	PIO1	O/I	SQI flash data 1 or config pin	
29 (F7)	PIO5	O/I	SQI flash chip select or CONFIG-SEL pins	
30 (H8)	PIO3	O/I	SQI flash data 3 or config pin	
31 (E6)	PIO8			
32 (F6)	PIO9			
33 (F5)	PIO10	I	D-SEL pin, Selection of Interface	Open=UART and DDC, GND=SPI
34 (H6)	PIO12	I	SAFEBOOT_N pin, to enter Safe Boot Mode	It is recommended to have a testpoint at SAFEBOOT_N pin, especially if SQI flash is used
35 (H7)	PIO11	O	TIMEPULSE1, 1PPS	Leave open if not used.
36 (F4)	PIO15	O	Antenna supervisor ANT_OFF	Leave open if not used.
37 (E4)	PIO16	I	Antenna supervisor ANT_OK	Leave open if not used.
38 (F3)	LDO_RF_OUT	O	RF domain voltage	Connect a 1.0uF capacitor to GND. Has to be used to supply VDD_ANA and VDD_LNA.
39 (H3)	VDD_LNA	I	Supply for LNA	Has to be supplied by LDO_RF_OUT, pin 38 (F3). It is recommended to add some filtering, see Figure 5.
40 (G1)	LNA_IN	I	RF input	
Body (B7, D1, D2, D3, D4, D5, D6, E5, F2, H2)	GND		GND	

Table 38: pin list

4.2 Schematic and bill of material design-in checklist

Power Supply:

- ☐ Low impedance, low ripple supply voltage is supplied to VDD_IO and V_CORE (<< 1 Ohm): Sections 2.1.2.1 and 2.1.2.2.
- ☐ Backup supply used or V_BCKP connected to VDD_IO: Section 2.1.2.3.
- ☐ Ferrite bead used to separate VDD_ANA and VDD_LNA from LDO_RF_OUT supply: Section 2.1.2.4.
- ☐ VDD_USB connected to GND if USB interface is not used: Section 2.7.
- ☐ Capacitor at LDO_X_OUT to GND has to be in place for crystal and TCXO designs: Section 2.4.
- ☐ System power supply is capable of delivering maximum current as specified in the UBX-G7020-Kx Data Sheet [1] and UBX-G7020-CT Data Sheet [2].

Interfaces:

- ☐ If SQI flash is used, part number is listed in section 3.4.
- ☐ Interface lines are protected from electromagnetic interference: Section 2.2.3.4
- ☐ A second serial interface is available for debugging at test-points: Section 2.2.3.

System functions:

- ☐ Real-Time clock circuit is present or not needed: Section 2.5.
- ☐ SAFEBOOT_N pin is accessible at a test-point: Section 2.2.6.
- ☐ Configuration pins (PIO0 to PIO5) are set as required by application (DCDC converter, LDO_X_OUT voltage): Section 2.2.2.
- ☐ SQI flash size and type are chosen correctly regarding application, means use of SQI flash (firmware and/or logging): Section 3.4.

RF section:

- ☐ Interference, ESD and RF power maximum rating issues have been addressed and the appropriate input circuit has been selected: Section 2.6.
- ☐ Use of additional external LNA has been evaluated based on required system performance: Section 2.6.2.2.
- ☐ A GPS/GNSS grade TCXO or crystal has been selected: Section 2.4, Table 13 and Table 15.
- ☐ Only COG, low tolerance capacitors are used in crystal circuit: Section 2.4.4.

4.3 Layout design-in checklist

General:

- ☐ Footprint for the u-blox 7 UBX-G7020 chip has been properly designed: Section 2.9.2
- ☐ RTC Crystal oscillator section is shielded by a GND guard ring: Section 2.9.1
- ☐ A proper GND concept is in place and solid GND plane and plenty of vias are being used for good RF GND connections: Section 2.9.1
- ☐ Power supply lines to V_CORE (or V_DCDC_IN in case of DCDC converter used) are wide and short and have plenty of vias to ensure low impedance: Section 2.1.2.1.
- ☐ In case feed-thru capacitors are being used, these are well connected to solid GND plane using plenty of vias.
- ☐ DCDC converter capacitor is well connected to GND and line from V_DCDC_OUT to V_VORE are short and wide.

RF Section:

- ☐ Crystal and/or TCXO are isolated from thermal gradients and air convection: Section 2.4 and 2.9.1

- ☐ GPS/GNSS Crystal oscillator section is shielded by a GND guard ring: Section 2.9.1
- ☐ RF signal lines are kept as short as possible and are designed as waveguides with proper impedance.

5 Production

5.1 Packaging, shipping, storage and moisture preconditioning

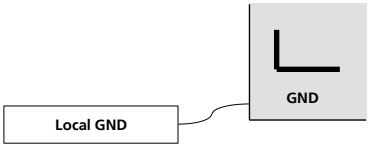
For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the UBX-G7020-Kx Data Sheet [1] and UBX-G7020-CT Data Sheet [2].

5.2 ESD handling precautions

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials in the vicinity of ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

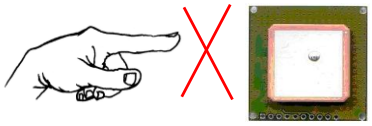
GPS receiver ICs are sensitive to ESD and require special precautions when handling. Particular care must be used when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver.

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB shall always be between the local GND and PCB GND.

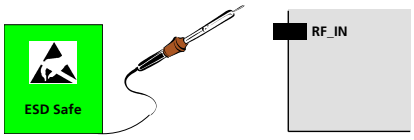


- When handling the RF-IC or placing components connected to the RF inputs or outputs, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10pF, coax cable ~50-80pF/m, soldering iron, …)

- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.



- When soldering components, make sure to use an ESD safe soldering iron (tip).



Failure to observe these precautions can result in severe damage to the GPS/GNSS receiver!

5.3 Soldering

Reflow soldering procedures are described in the IPC/JEDEC J-STD-020 standard.

5.4 Production

In production the first operation is to configure the UBX-G7020 properly as outlined below:

- Set the Low Level Configuration
- Program Firmware (for designs with SQI flash and not running from ROM firmware)
- Set the Functional Configuration

For details on how to set the configuration see section 2.10. Programming the SQI flash can be accomplished using either u-center (the u-blox GPS/GNSS evaluation software) or via a firmware update utility. A flowchart detailing the sequence for applying the configuration and programming the SQI flash is shown below in section 5.4.1.

When configured properly, the design has to be tested regarding its GPS/GNSS capability. See section 5.4.2.

Once running, monitoring of system parameters can be done via a PIO serial interface, see section 5.4.3.

5.4.1 Set the Low Level Configuration and program the optional SQI flash

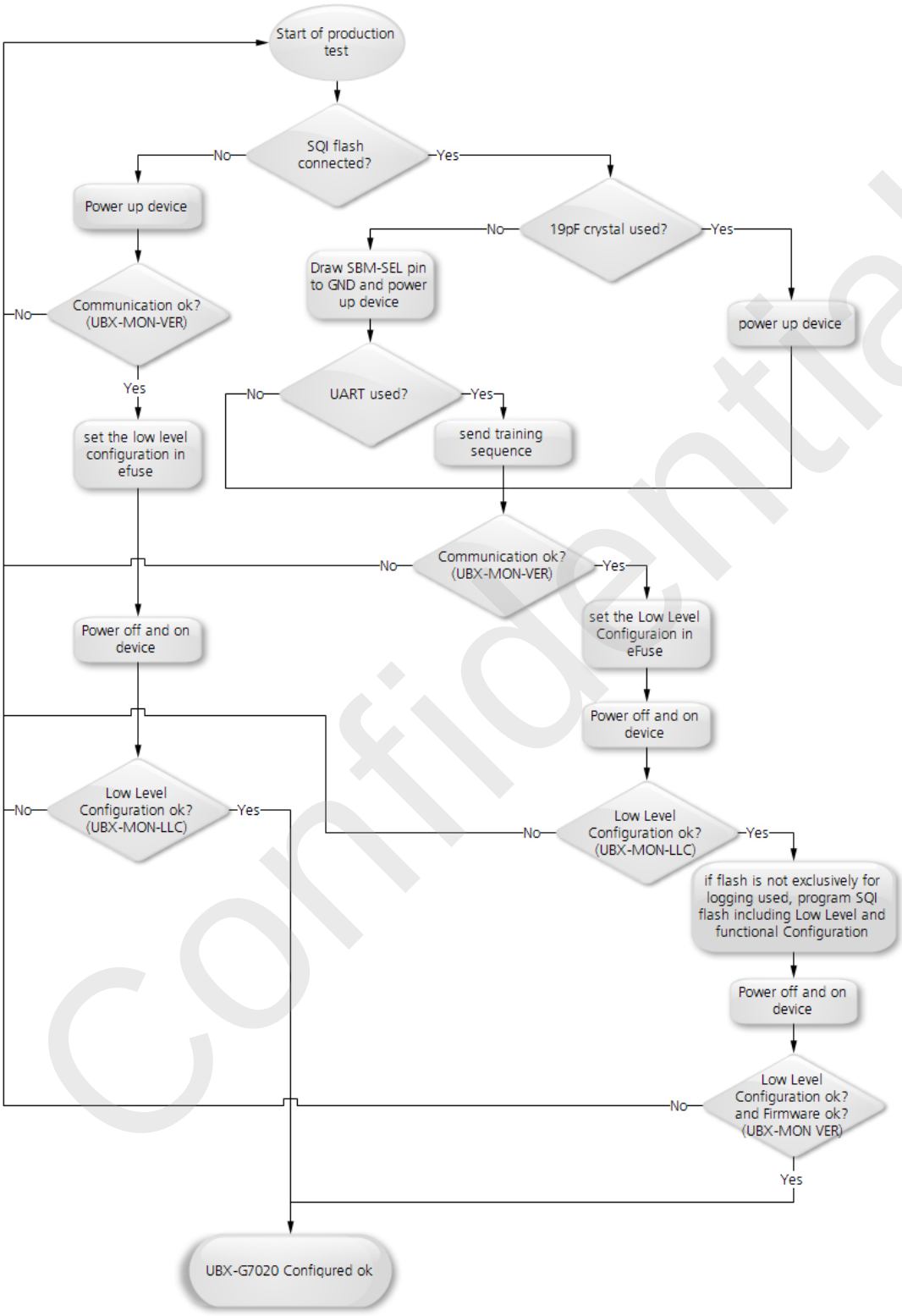


Figure 28: Sequence in production to set the Low Level Configuration and program the optional SQI flash

5.4.2 Test the GPS/GNSS performance

A standard in-circuit production test for the user application will use the UBX-MON-PT protocol message and will need access to a serial interface, e.g. DDC, SPI or UART. See the u-blox 7 Receiver Description including Protocol Specification [3] for the description of the UBX-MON-PT production test message. If PIO13 (EXTINT0 pin) is also accessible in production test, time aiding may be used in order to reduce test time. This is also described in the u-blox 7 Receiver Description including Protocol Specification [3].

Value	Description	Min.	Typ.	Max.	Comments
Pgain	PGA gain		~80		Gives indication about the gain of the whole RF path. If external LNA or active antenna used, the value becomes lower.
dopplerMin and dopplerMax - if TCXO is used - if crystal is used	Doppler	 - 4000 Hz - 19000 Hz		 + 4000 Hz + 19000 Hz	It is mandatory that the frequency of the TCXO/ crystal is within these limits. Make sure that the used single channel simulator has no doppler offset.
carrphDevMax	Carrier Phase Deviation		0.004		Gives some information about the stability of the crystal/TCXO. 0.004 is the typical value for a tracked SV with C/No ratio of about 40dB*Hz. For lower C/No the value becomes higher.
cnoMin and cnoMax	C/No ratio		40 dBHz		
postStatus	Power on self test	0x00000000		0x00000000	

Table 39: Limits for UBX-MON-PT measurements

5.4.3 System monitoring

The u-blox 7 GPS Receiver provides System Monitoring functions that allow the operation of the embedded processor and associated peripherals to be supervised. These System Monitoring functions are output as part of the UBX protocol, class 'MON'.

Please refer to the u-blox 7 Receiver Description including Protocol Specification [3] for more information on UBX messages, serial interfaces for design analysis and individual system monitoring functions.

Appendix

A Reference schematics

A.1 Cost optimized circuit

- Firmware runs out of ROM
- Passive antenna
- Crystal
- Single crystal feature used (RTC derived from main clock)
- UART and DDC for communication to host

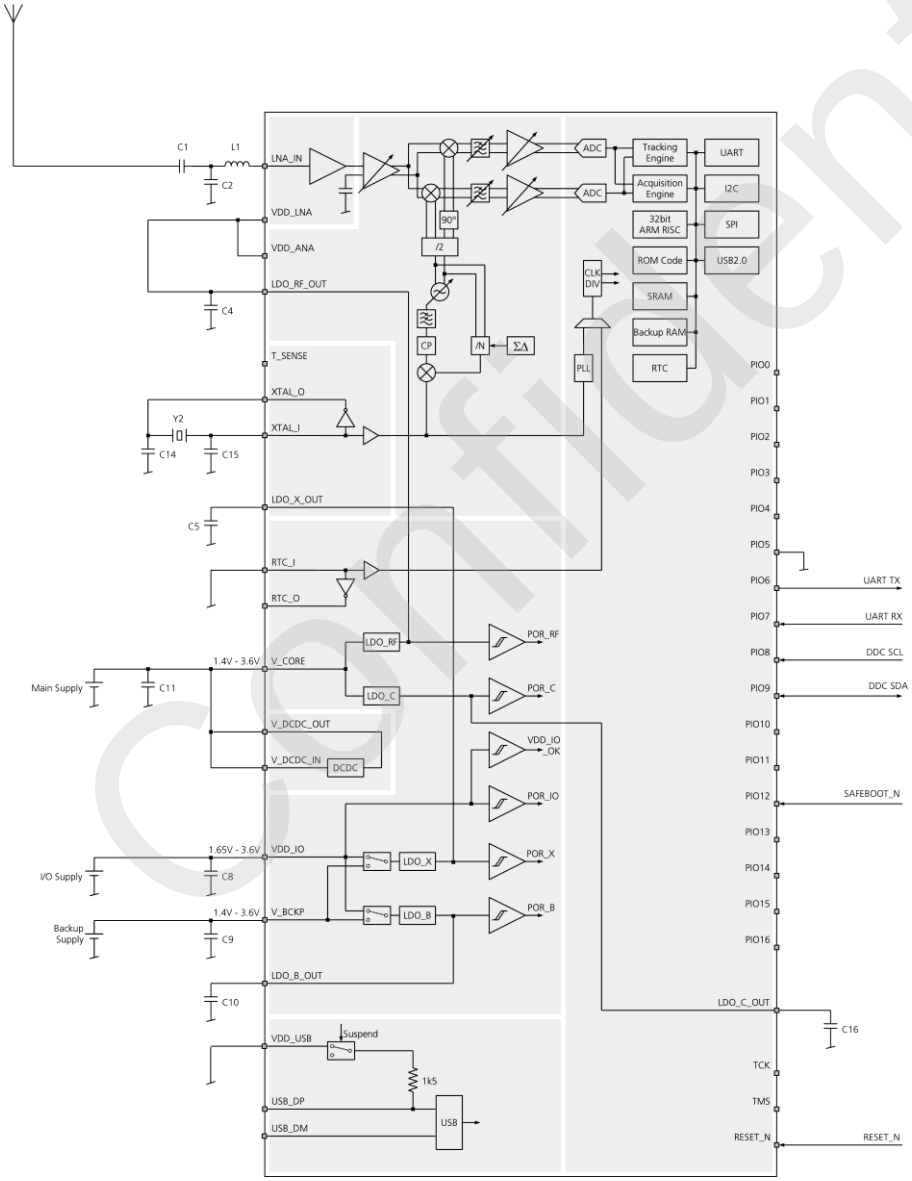


Figure 29: Cost optimized circuit

A.2 Best performance circuit

- 1.8V TCXO supplied by LDO_X_OUT
- External LNA
- RTC crystal
- Filtering for LNA supply
- UART and DDC interface

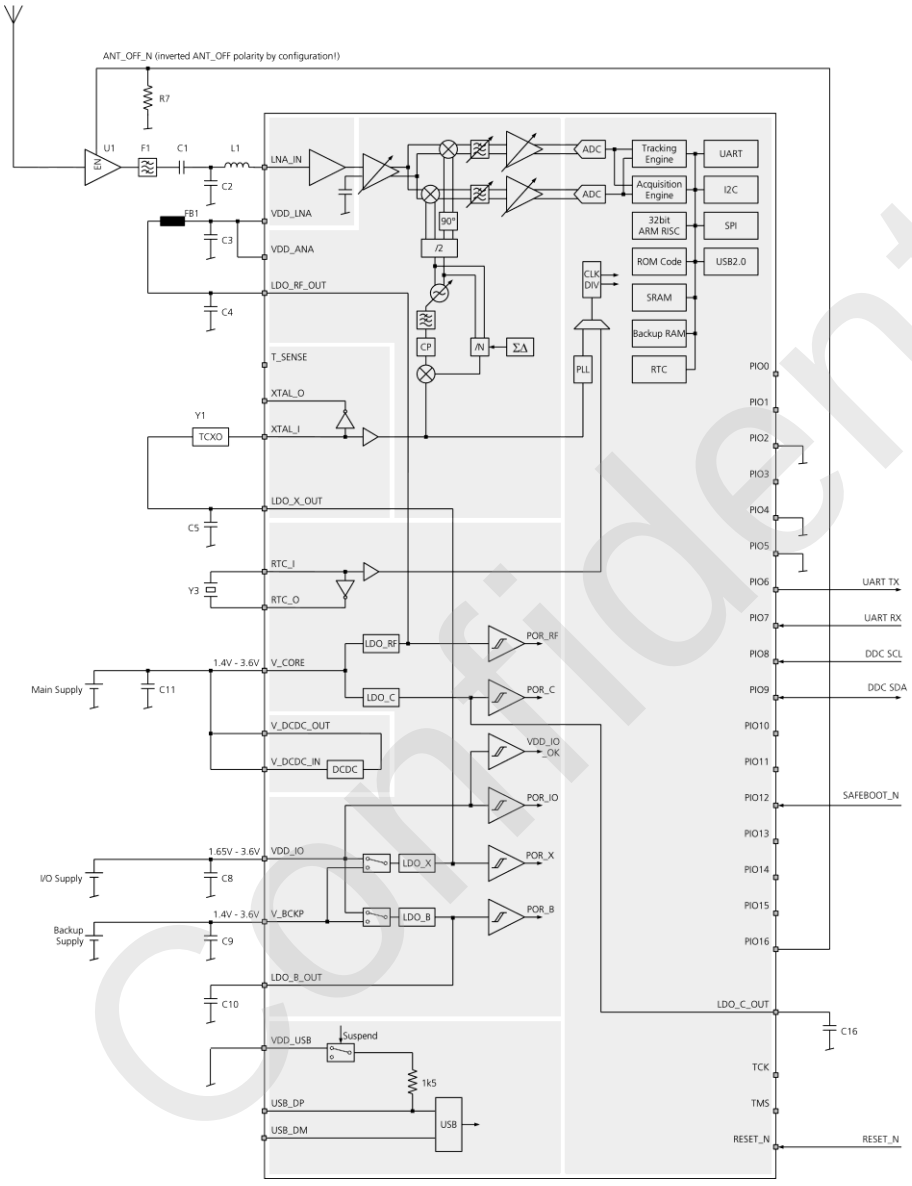


Figure 30: Best performance circuit

VDD_IO supply must be higher than 2.1V because of 1.8V TCXO used.

A.3 Power optimized circuit

- DCDC converter
- Crystal
- RTC crystal
- SPI interface
- No SQI flash

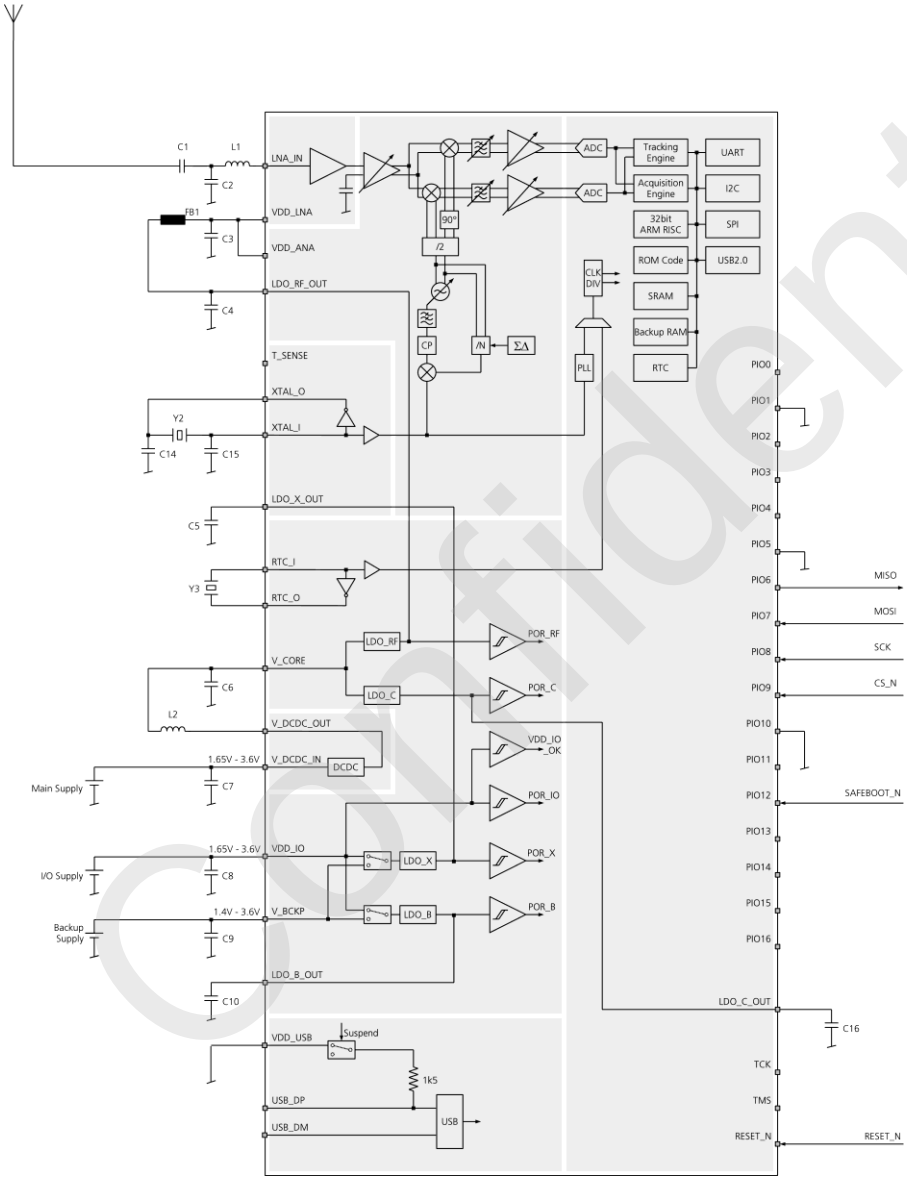


Figure 31: Power optimized circuit

A.4 Improved jamming immunity

- External SAW filter – LNA – SAW filter
- DCDC converter
- 1.8V TCXO supplied by LDO_X_OUT
- RTC crystal
- UART and DDC interface

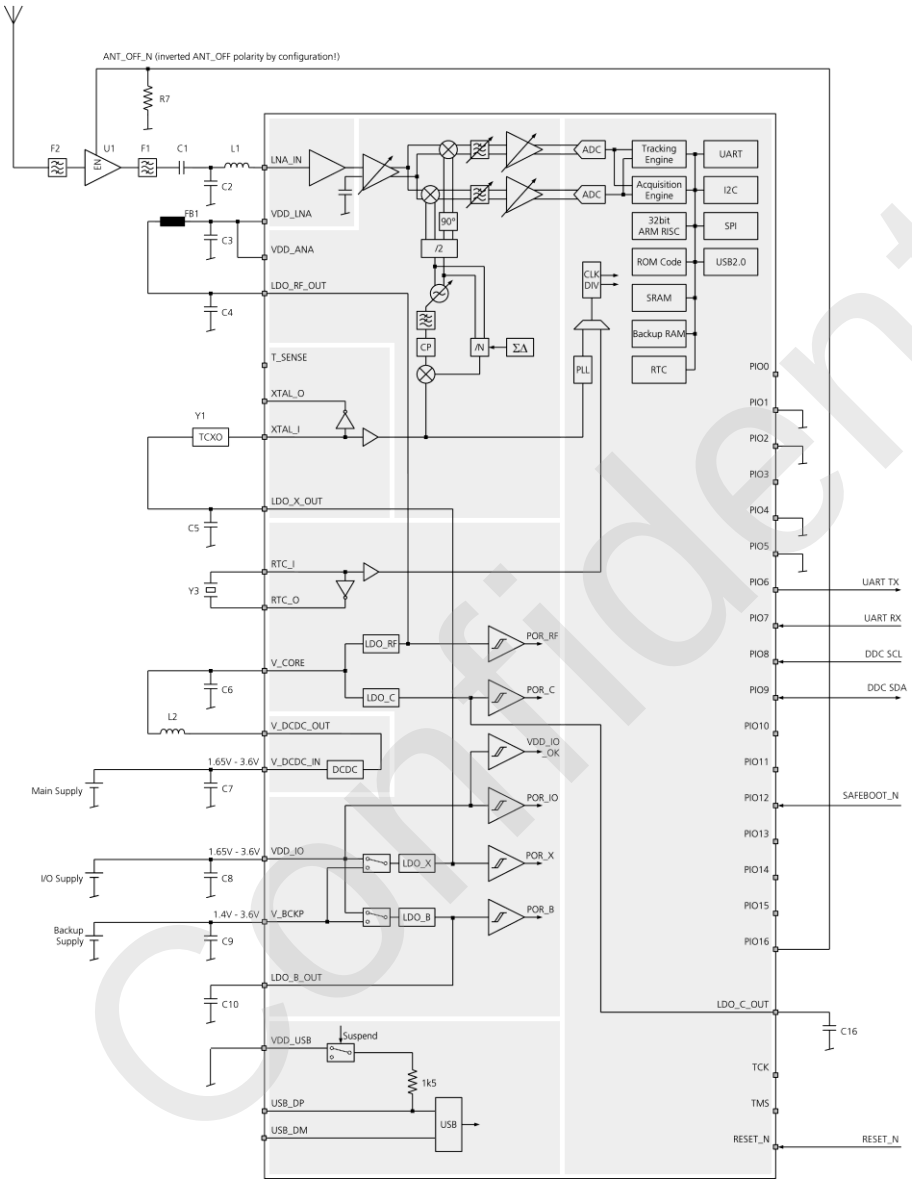


Figure 32: Standard circuit for an improved jamming immunity

VDD_IO supply must be higher than 2.1V because of 1.8V TCXO used.

A.5 1.8V design using TCXO

- 1.8V TCXO
- UART and DDC interface
- RTC crystal
- UART and DDC interface
- External LNA

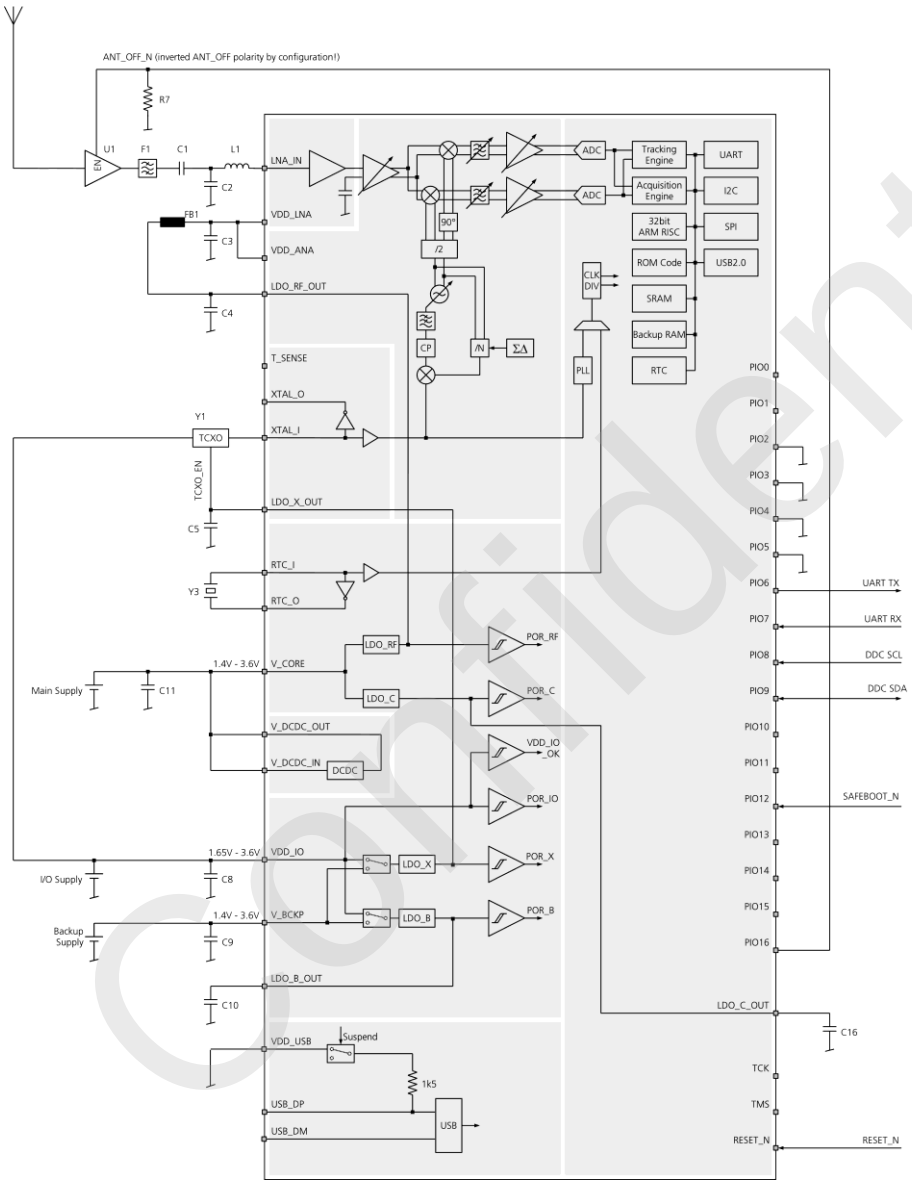


Figure 33: Standard circuit using the SPI interface

A.6 Circuit using active antenna

- Active antenna
- 3V TCXO
- UART and DDC
- RTC crystal

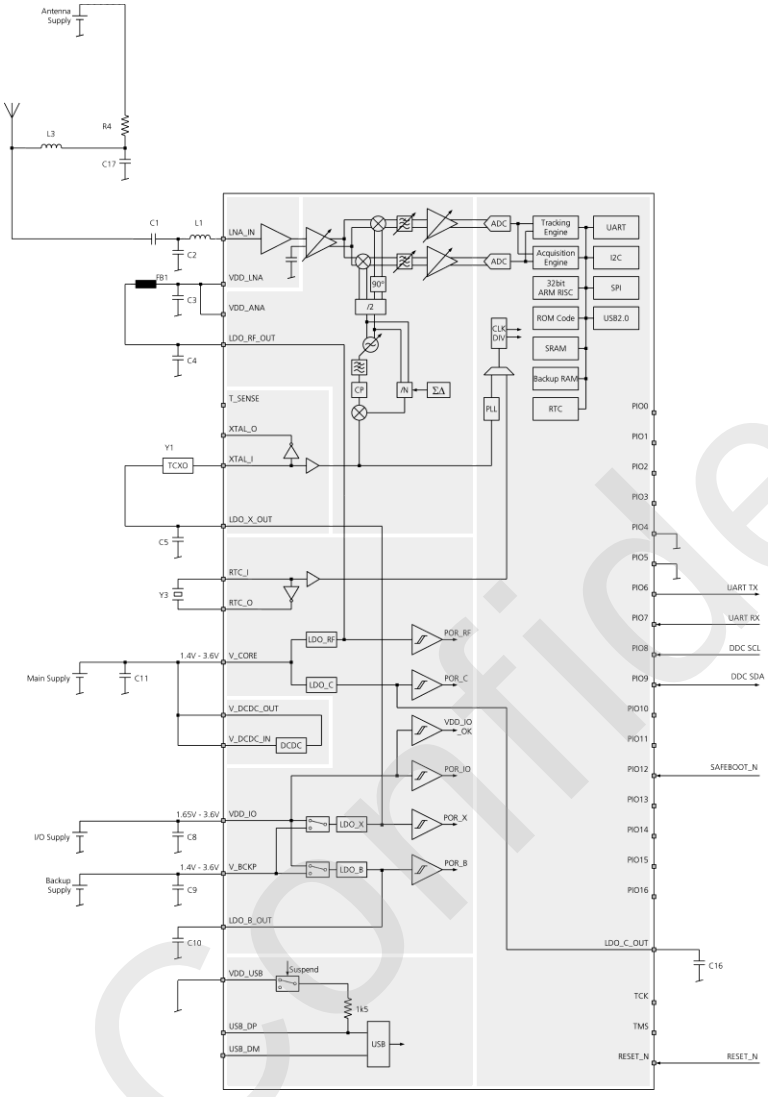


Figure 34: Standard circuit using active antenna

VDD_IO supply must be higher than 3.2V because of 3V TCXO used.

A.7 USB self-powered circuit

- 1.8V TCXO
- USB
- External LNA
- RTC
- SQI flash

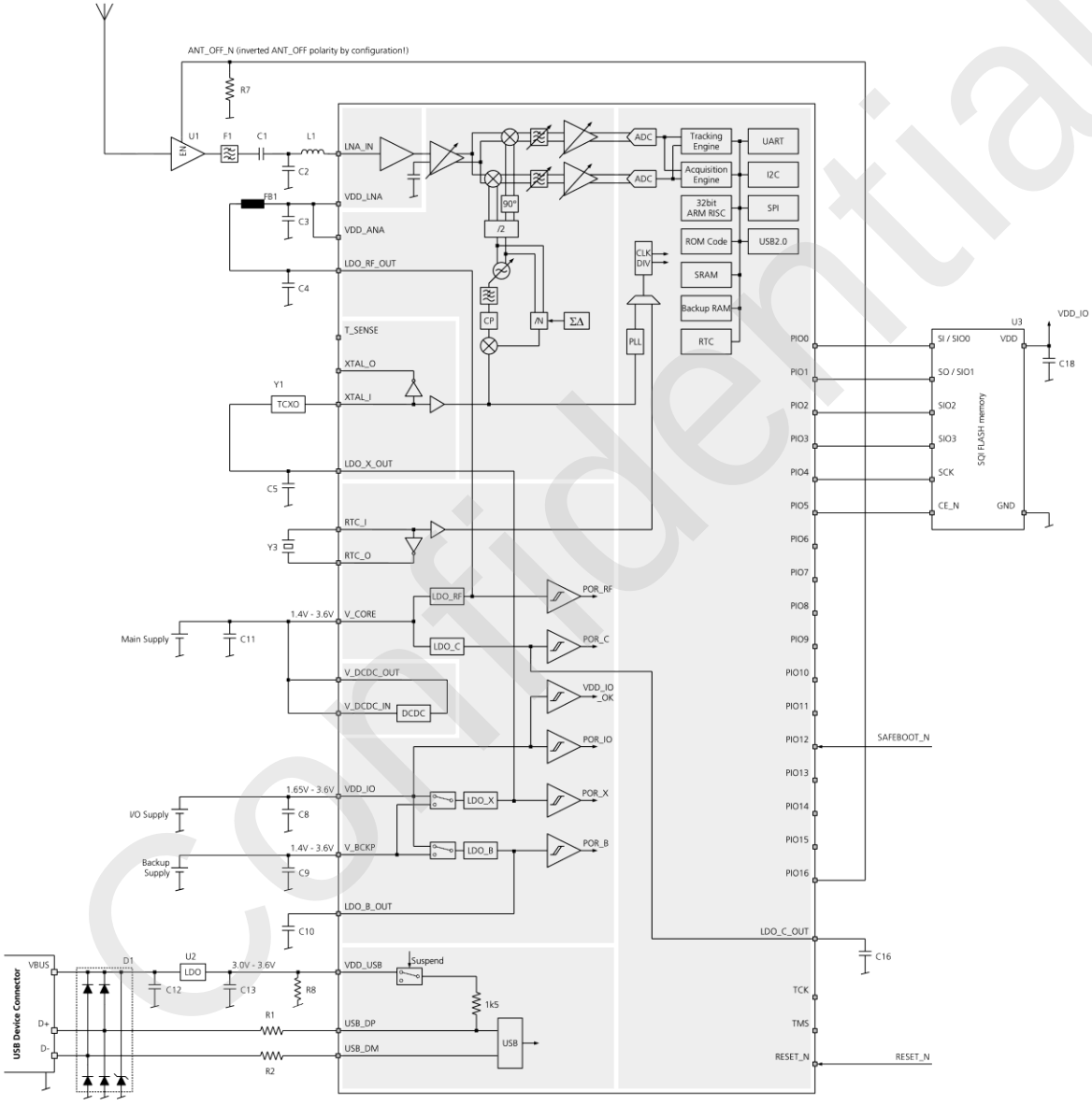


Figure 35: USB self-powered circuit

☞ VDD_IO supply must be higher than 2.1V because of 1.8V TCXO used.

A.8 USB bus-powered circuit

- 1.8V TCXO
- USB
- DCDC converter
- External LNA
- RTC
- SQI flash

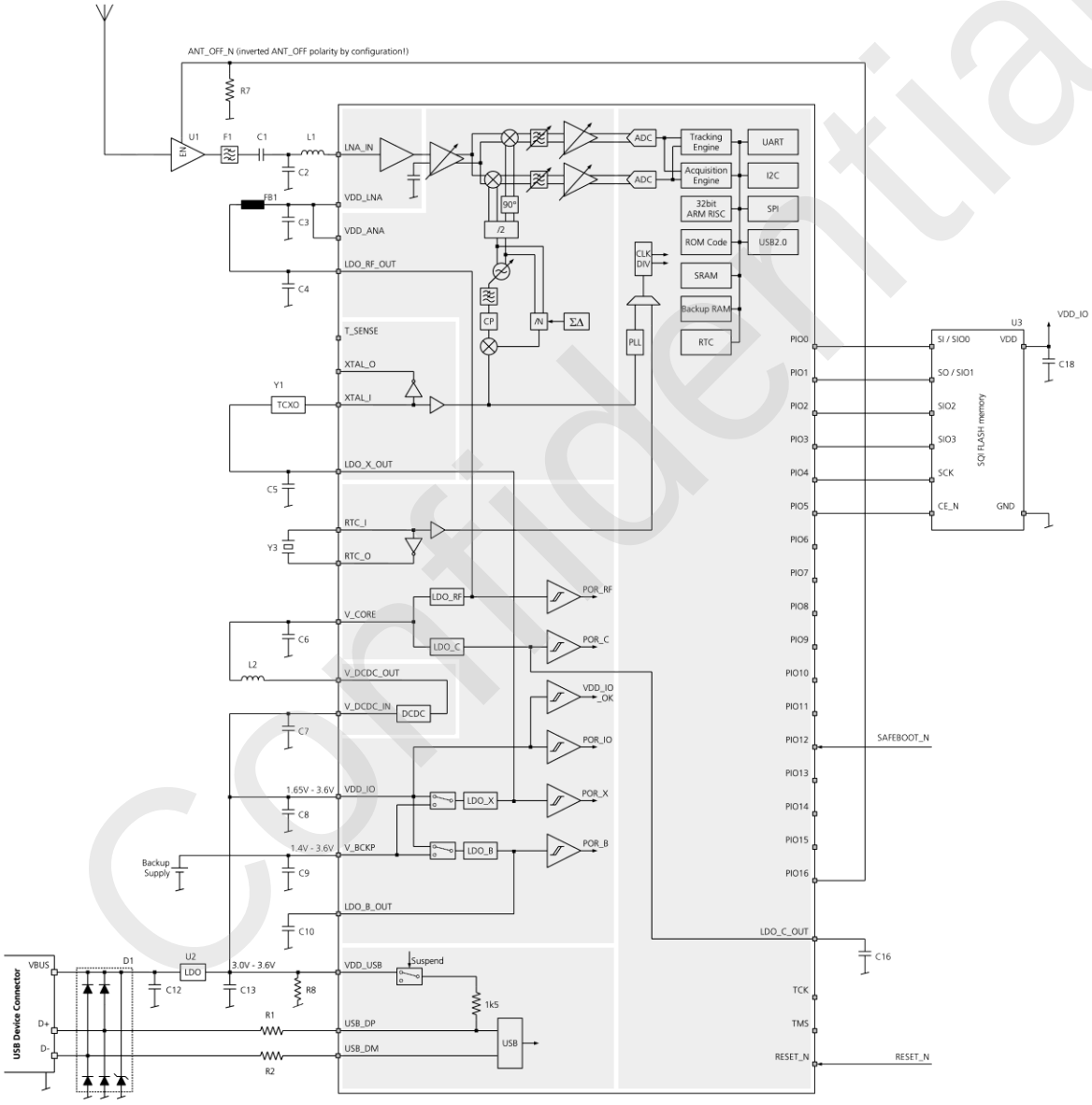


Figure 36: USB bus-powered circuit

A.9 Circuit using 3-pin antenna supervisor

- 3-pin antenna supervisor
- RTC
- Crystal
- UART and DDC interface
- SQI flash

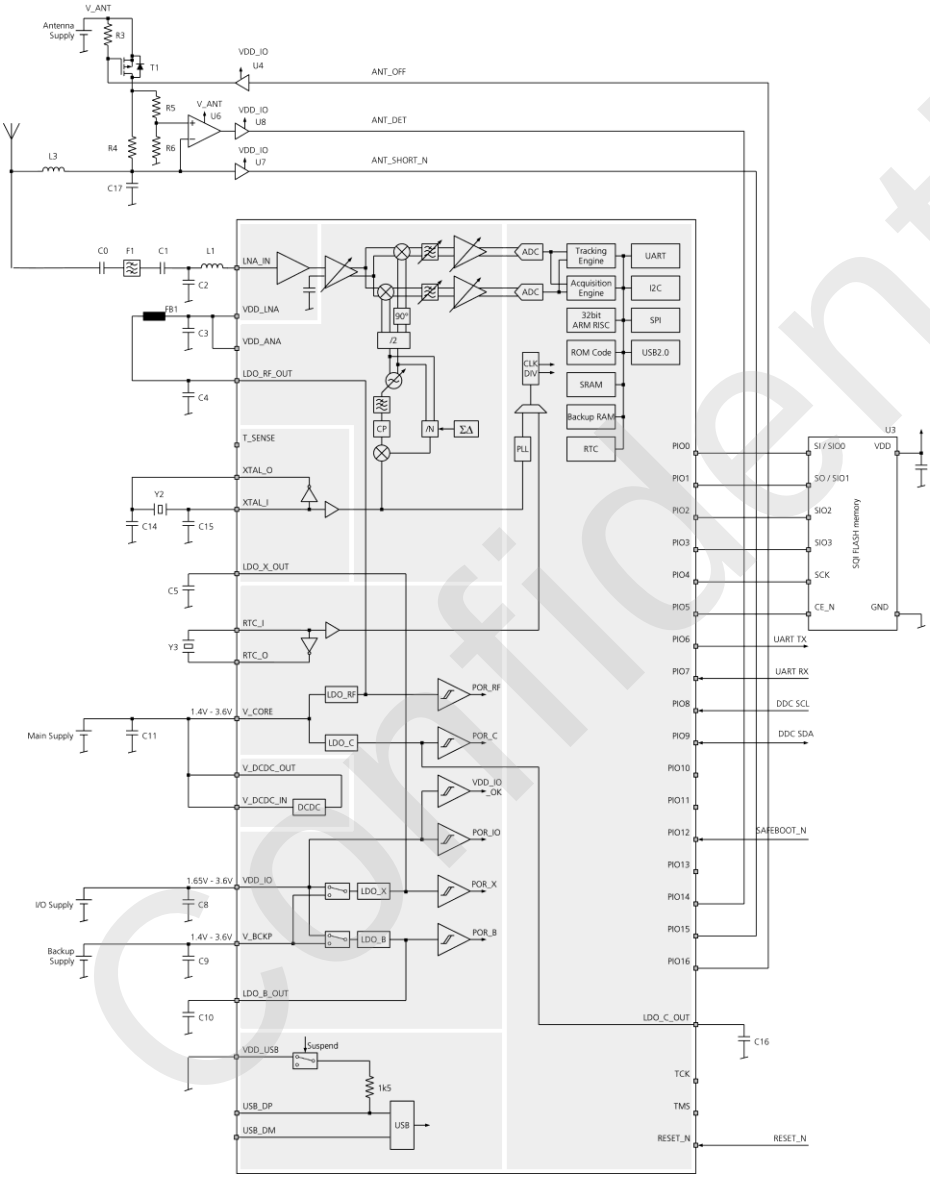


Figure 37: Circuit using 3-pin antenna supervisor

Related documents

[1] UBX-G7020-Kx Data Sheet, Docu. No. GPS.G7-HW-12001

[2] UBX-G7020-CT Data Sheet, Docu. No. GPS.G7-HW-12002

[3] u-blox 7 Receiver description including protocol specification, Docu. No. GPS.G7-SW-12002

[4] http://www.murata.com/products/emc/knowhow/index.html

[5] http://www.murata.com/products/emc/knowhow/pdf/4to5e.pdf

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

Revision history

Revision	Date	Name	Status / Comments
-	05/07/2012	mdur	Objective Specification

Contact

For complete contact information visit us at www.u-blox.com

Headquarters

u-blox AG

Zuercherstrasse 68
CH-8800 Thalwil
Switzerland

Phone: +41 44 722 74 44
Fax: +41 44 722 74 47
E-mail: info@u-blox.com

Offices

North, Central and South America

u-blox America, Inc.

Phone: +1 (703) 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:

Phone: +1 (703) 483 3184
E-mail: info_us@u-blox.com

Technical Support:

Phone: +1 (703) 483 3185
E-mail: support_us@u-blox.com

Europe, Middle East, Africa

u-blox AG

Phone: +41 44 722 74 44
E-mail: info@u-blox.com

Technical Support:

Phone: +41 44 722 74 44
E-mail: info@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.

Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office China:

Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office Japan:

Phone: +81 3 4360 5343
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:

Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:

Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com