36V, 2μA I_Q, 200mA Low Dropout Voltage Linear Regulator

General Description

The RT9069 is a low-dropout (LDO) voltage regulators with enable function offering the benefits of high input voltage, low-dropout voltage, low-power consumption, and miniaturized packaging.

The features of low quiescent current as low as 2μA and zero disable current is ideal for powering the battery equipment to a longer service life. The RT9069 is stable with the ceramic output capacitor over its wide input range from 3.5V to 36V and the entire range of output load current (0mA to 200mA).

Applications

- Portable, Battery Powered Equipments
- Extra Low Voltage Microcontrollers
- Notebook Computers

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Features

- **2μA Ground Current at no Load**
- **±2% Output Accuracy**
- **200mA Output Current with EN**
- **Zero Disable Current**
- **Maximum Operating Input Voltage 36V**
- **Dropout Voltage: 0.2V at 10mA/ VIN 5V**
- **Support Fixed Output Voltage 2.5V, 3V, 3.3V, 5V, 9V, 12V**
- **Stable with Ceramic or Tantalum Capacitor**
- **Current Limit Protection**
- **Over-Temperature Protection**
- **RoHS Compliant and Halogen Free**

Ordering Information

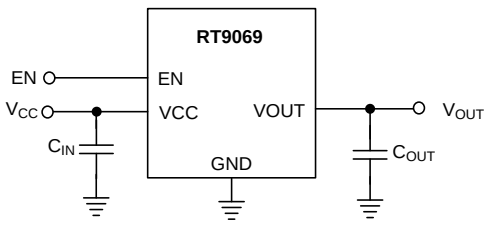
RT9069-□□□□

Package Type
SP : SOP-8 (Exposed Pad-Option 1)
B : SOT-23-5
X5 : SOT-89-5
QU : UDFN-6L 1.6x1.6 (U-type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

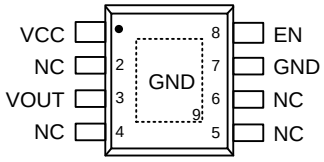
Output Voltage
25 : 2.5V
30 : 3V
33 : 3.3V
50 : 5V
90: 9V
C0: 12V
Special Request: Any Voltage between 2.5V and 12V under specific business agreement

Simplified Application Circuit

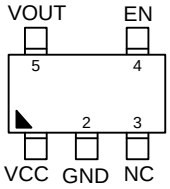


Pin Configurations

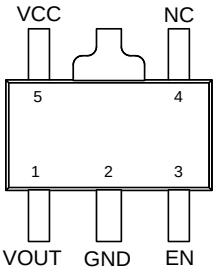
(TOP VIEW)



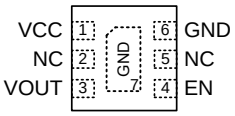
SOP-8 (Exposed Pad)



SOT-23-5



SOT-89-5

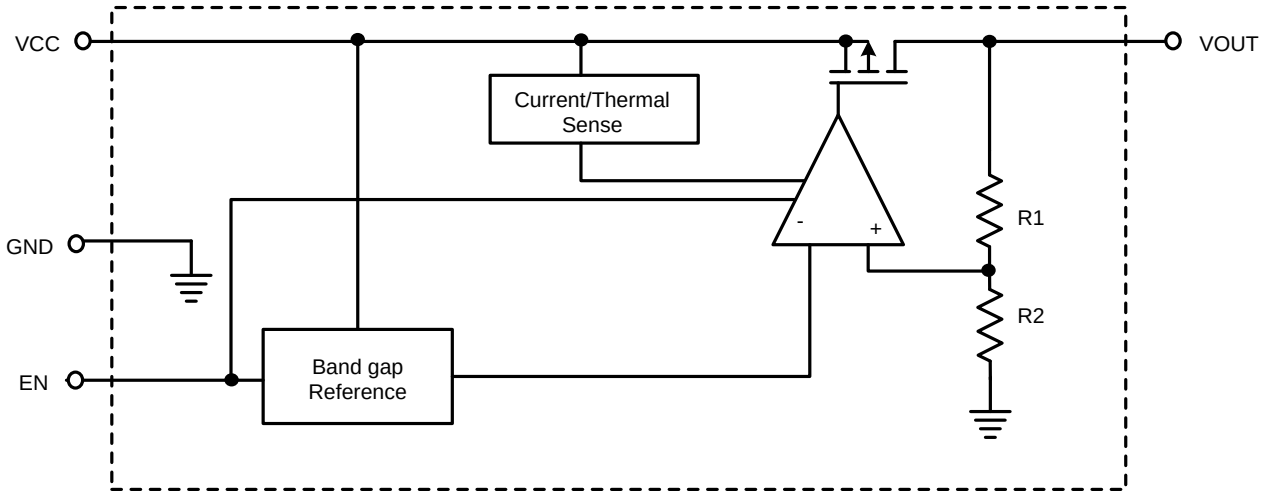


UDFN-6L 1.6x1.6

Functional Pin Description

Pin No.				Pin Name	Pin Function
SOP-8 (Exposed Pad)	SOT-23-5	SOT-89-5	UDFN-6L 1.6x1.6		
1	1	5	1	VCC	Supply Voltage Input.
2, 4, 5, 6	3	4	2, 5	NC	No Internal Connection.
3	5	1	3	VOUT	Output of the Regulator.
7, 9 (Exposed Pad)	2	2	6, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
8	4	3	4	EN	Enable Control Input.

Function Block Diagram



Operation

Basic Operation

The RT9069 is a high input voltage linear regulator designed especially for low external component systems. The input voltage range is from 3.5V to 36V. The minimum required output capacitance for stable operation is 1μF effective capacitance after consideration of the temperature and voltage coefficient of the capacitor.

Output Transistor

The RT9069 builds in a P-MOSFET output transistor which provides a low switch-on resistance for low dropout voltage applications.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

Enable

The RT9069 delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is zero.

Current Limit Protection

The RT9069 provides current limit function to prevent the device from damages during over-load or shorted-circuit conditions. This current is detected by an internal sensing transistor.

Over-Temperature Protection

The over-temperature protection function turns off the P-MOSFET when the junction temperature exceeds 150°C (typ.) and the output current exceeds 4mA. Once the junction temperature cools down by approximately 20°C, the regulator automatically resumes operation.

Absolute Maximum Ratings (Note 1)

- VCC, EN to GND ---------- –0.3V to 40V
- VOUT to VCC ---------- –40V to 0.3V
- VOUT to GND
  - RT9069-90/RT9069-C0 ---------- –0.3V to 15V
  - RT9069-25/RT9069-30/RT9069-33/RT9069-50 ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 (Exposed Pad) ---------- 3.26W
  - SOT-23-5 ---------- 0.45W
  - SOT-89-5 ---------- 0.87W
  - UDFN-6L 1.6x1.6 ---------- 2.15W
- Package Thermal Resistance (Note 2)
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 30.6°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 3.4°C/W
  - SOT-23-5, θ_{JA} ---------- 218.1°C/W
  - SOT-23-5, θ_{JC} ---------- 28.5°C/W
  - SOT-89-5, θ_{JA} ---------- 113.9°C/W
  - SOT-89-5, θ_{JC} ---------- 6.9°C/W
  - UDFN-6L 1.6x1.6, θ_{JA} ---------- 46.5°C/W
  - UDFN-6L 1.6x1.6, θ_{JC} ---------- 18.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 3.5V to 36V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, C_{IN} = 1μF, T_A = 25°C, for each LDO unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3.5	--	36	V
Output Voltage Range	V_{OUT}		2.5	--	12	V
DC Output Accuracy	ΔV_{OUT}	I_{LOAD} = 10mA	–2	--	+2	%
Dropout Voltage	V_{DROP}	I_{LOAD} = 10mA, V_{CC} > 5V	--	0.2	0.36	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} Consumption Current		I_Q	I_{LOAD} = 0mA, $V_{OUT} \leq$ 5.5V	--	2	3.5	μA
			I_{LOAD} = 0mA, V_{OUT} > 5.5V, V_{CC} =15V	--	3.5	5	μA
Shutdown Current			V_{EN} = 0V	--	0.1	--	μA
Shutdown Leakage Current			V_{EN} = 0V, V_{OUT} = 0V	--	0.1	--	μA
EN Input Current		I_{EN}	V_{EN} = 36V	--	0.1	--	μA
Line Regulation		ΔV_{LINE}	I_{LOAD} = 1mA, V_{OUT} +1 < V_{CC} < 36V, V_{OUT} > 3.3V	--	0.04	0.5	%
			I_{LOAD} = 1mA, V_{OUT} +1 < V_{CC} < 36V, $V_{OUT} \leq$ 3.3V	--	0.04	0.6	
Load Regulation		ΔV_{LOAD}	0mA < I_{LOAD} < 100mA	–1	--	1	%
Output Current Limit		I_{LIM}	V_{OUT} = 0.5 x $V_{OUT(normal)}$	200	350	--	mA
Enable Input Voltage	Logic-High	V_{IH}		--	--	2	V
	Logic-Low	V_{IL}		0.6	--	--	
Thermal Shutdown Temperature		T_{SD}	I_{LOAD} = 30mA	--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

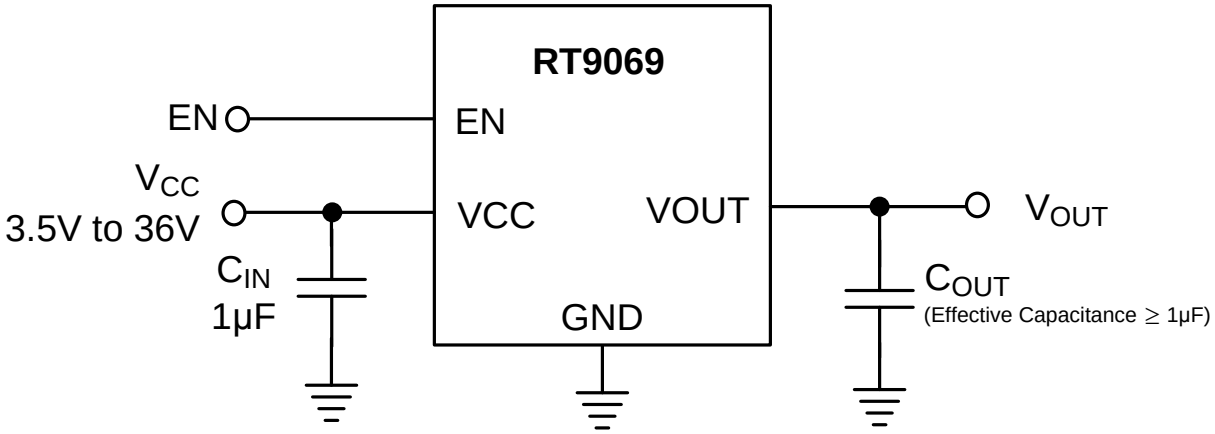
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

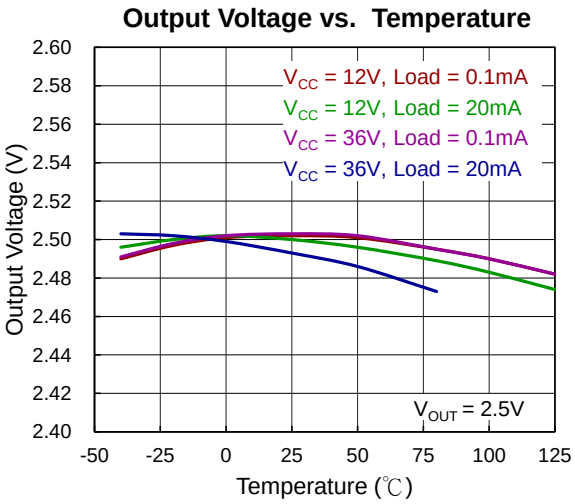
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

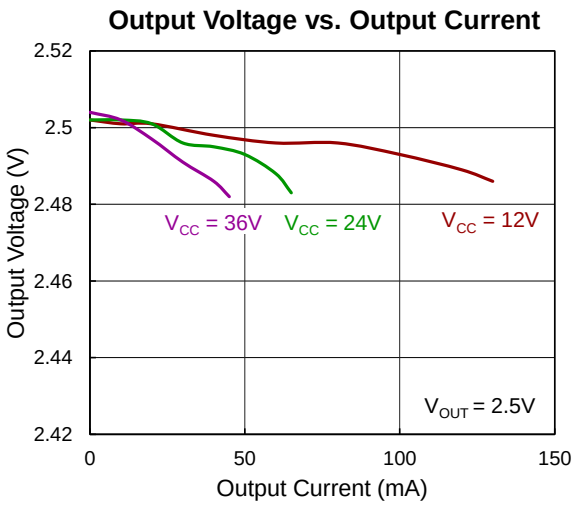
Note 4. The device is not guaranteed to function outside its operating conditions.

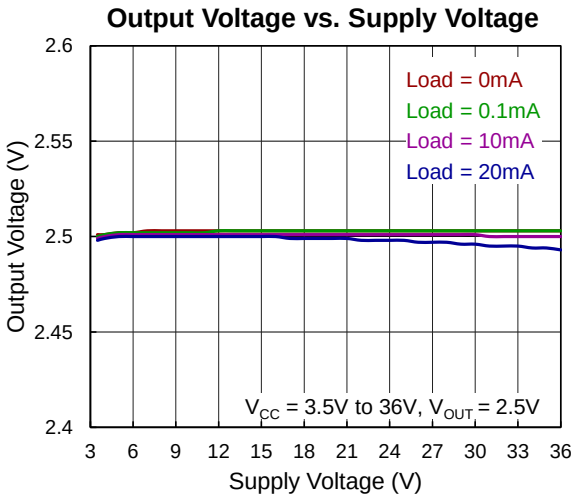
Typical Application Circuit

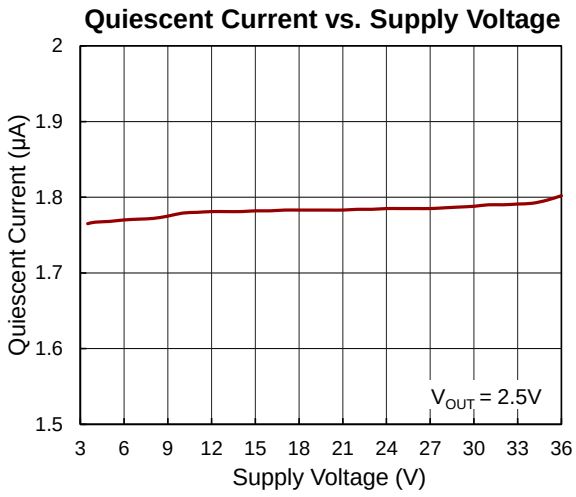


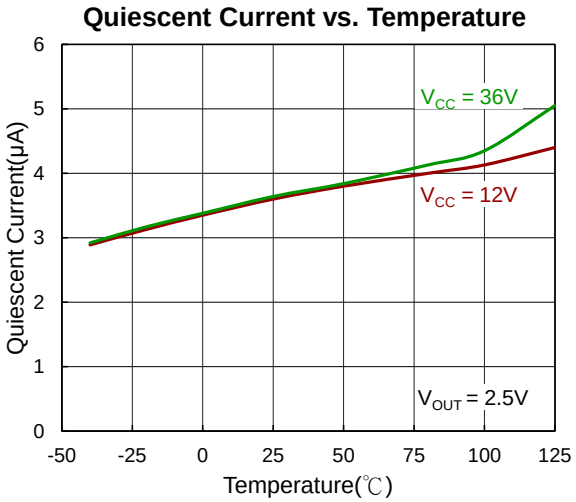
Typical Operating Characteristics

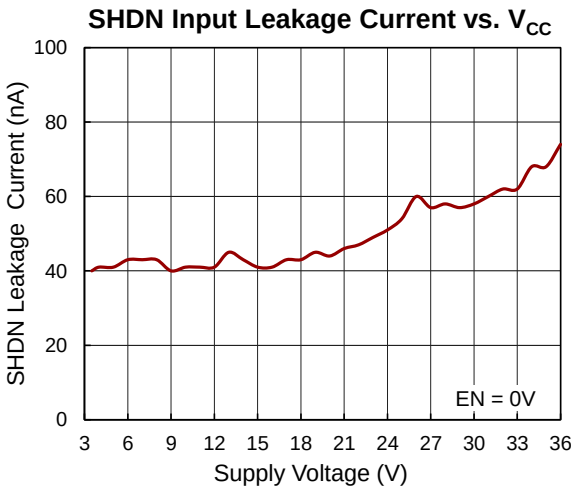




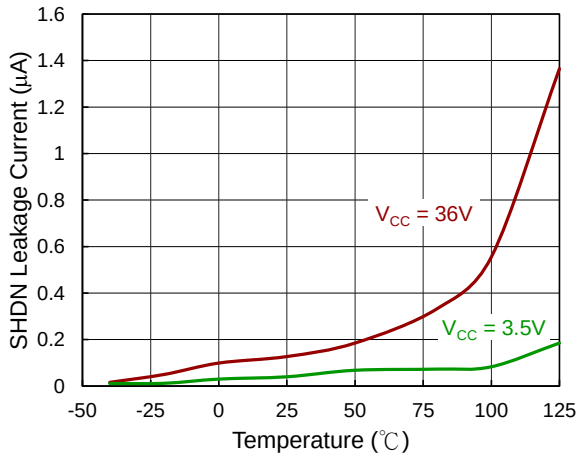




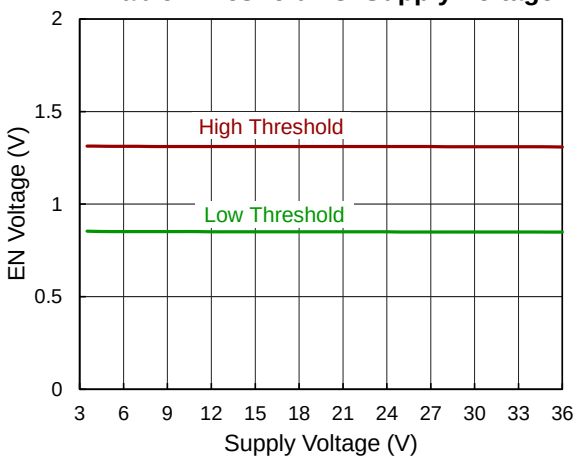




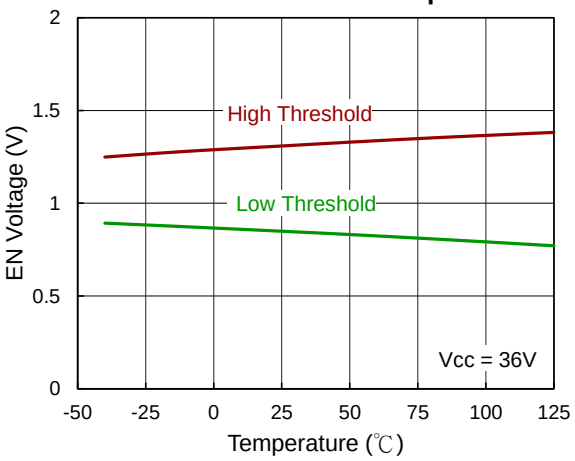
SHDN Leakage Input Current vs. Temp.



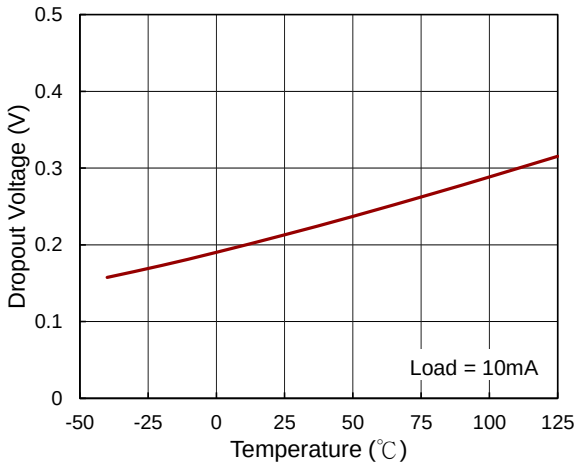
Enable Threshold vs. Supply Voltage



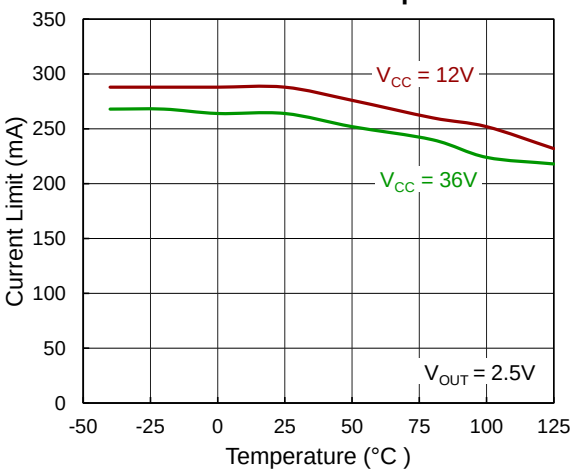
Enable Threshold vs. Temperature



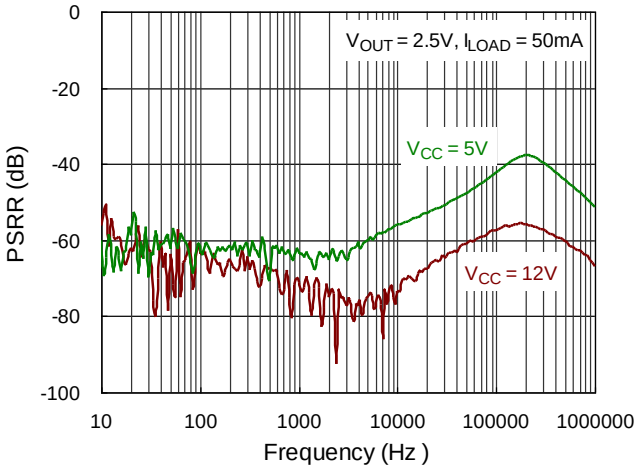
Dropout Voltage vs. Temperature



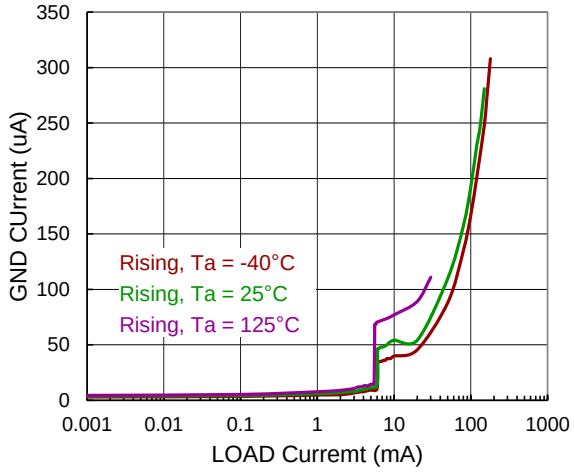
Current Limit vs. Temperature



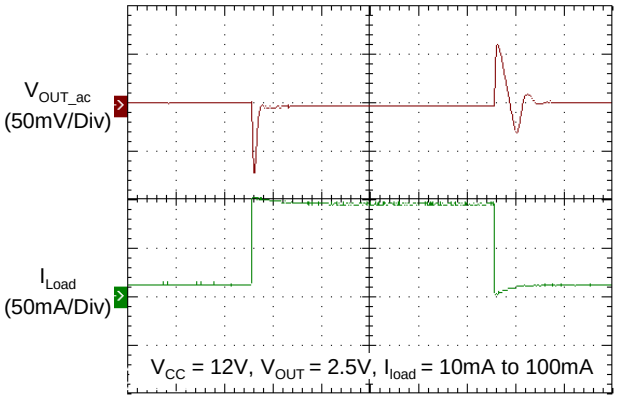
PSRR vs. Frequency



Ground Current vs. Load Current

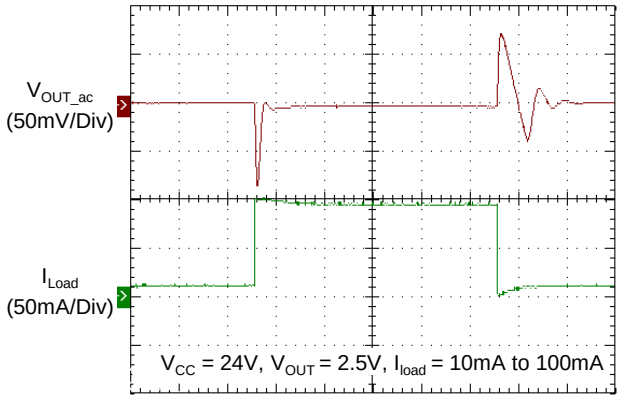


Load Transient Response



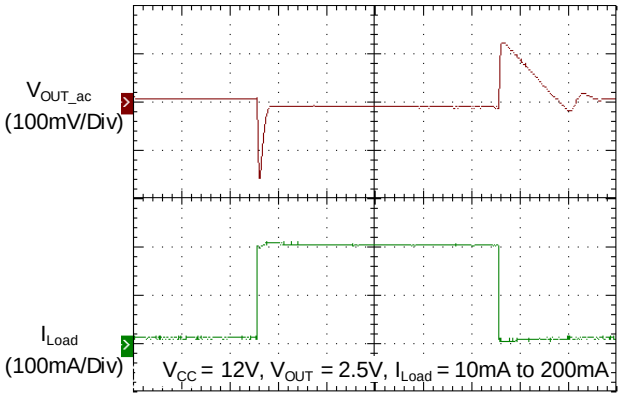
Time (250μs/Div)

Load Transient Response



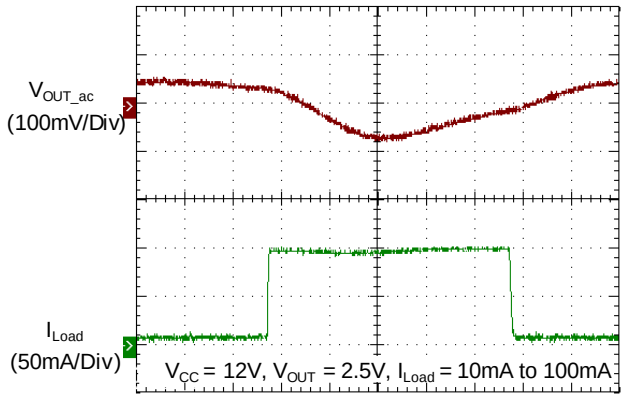
Time (250μs/Div)

Load Transient Response



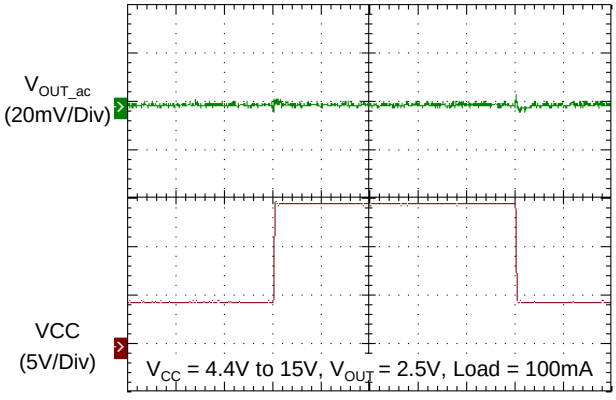
Time (250μs/Div)

Load Transient Response



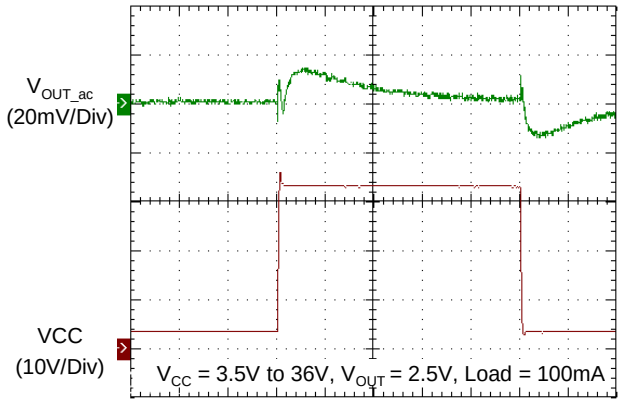
Time (10μs/Div)

Line Transient Response



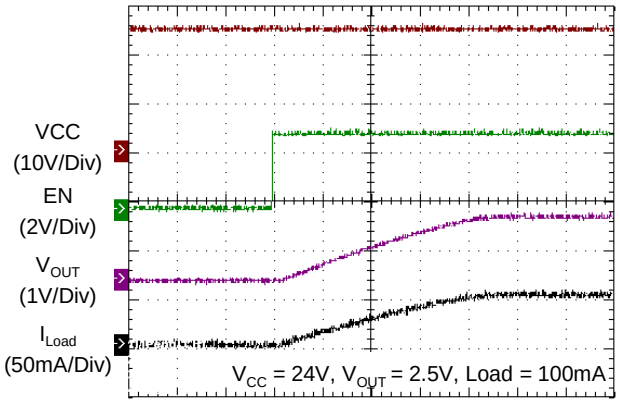
Time (100μs/Div)

Line Transient Response



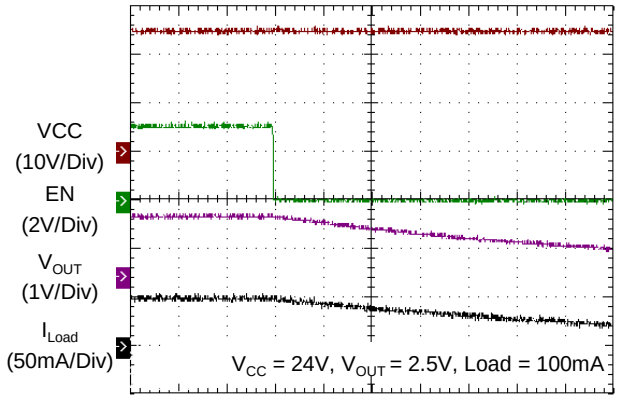
Time (100μs/Div)

Power On from EN



Time (25μs/Div)

Power Off from EN



Time (25μs/Div)

Application Information

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance, θ_{JA}, is 30.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOT-23-5 package, the thermal resistance, θ_{JA}, is 218.1°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOT-89-5 package, the thermal resistance, θ_{JA}, is 113.9°C/W on a standard JEDEC 51-7 four-layer thermal test board. For UDFN-6L 1.6x1.6 package, the thermal resistance, θ_{JA}, is 46.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.6°C/W) = 3.2679W for SOT-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (218.1°C/W) = 0.4585W for SOT-23-5 package

$P_{D(MAX)}$ = (125°C – 25°C) / (113.9°C/W) = 0.8779W for SOT-89-5 package

$P_{D(MAX)}$ = (125°C – 25°C) / (46.5°C/W) = 2.15W for UDFN-6L 1.6x1.6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation

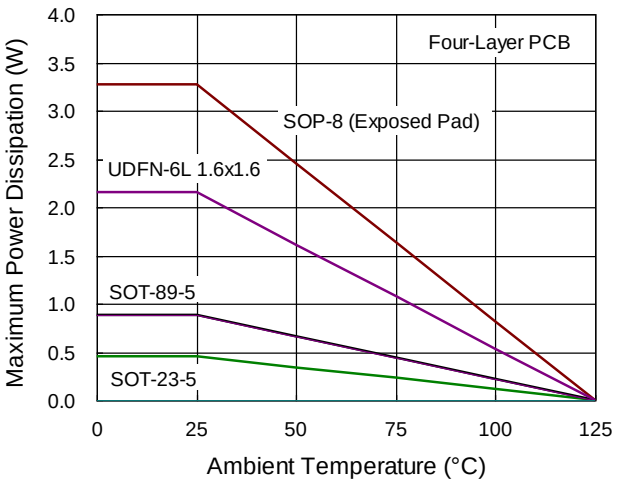
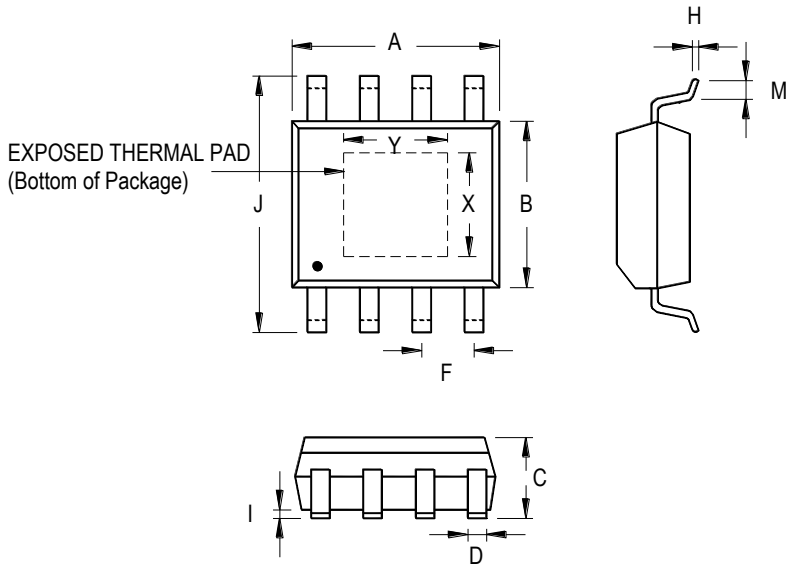


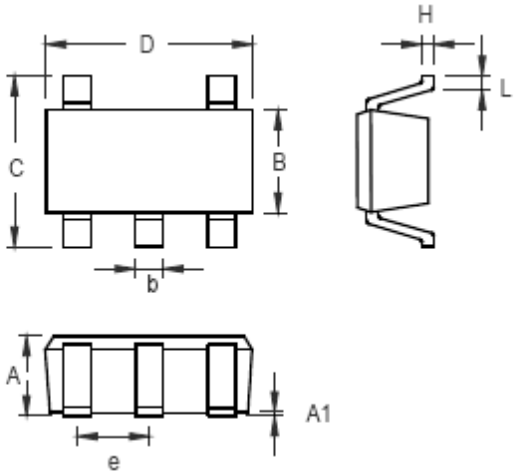
Figure 1. Derating Curve of Maximum Power Dissipation

Outline Dimension



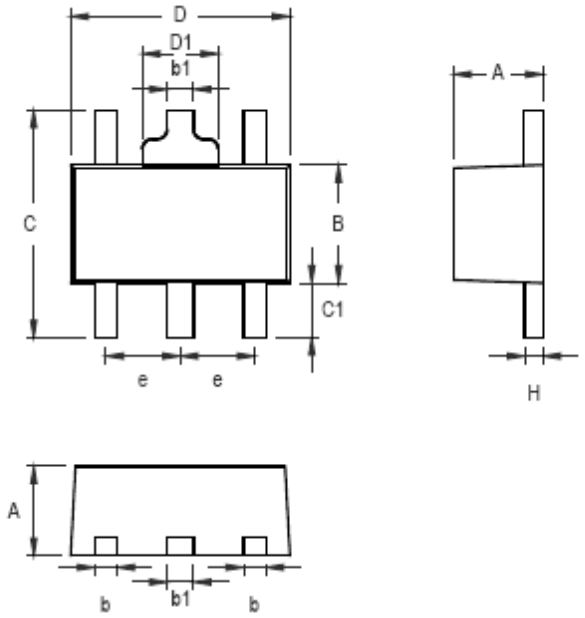
Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package



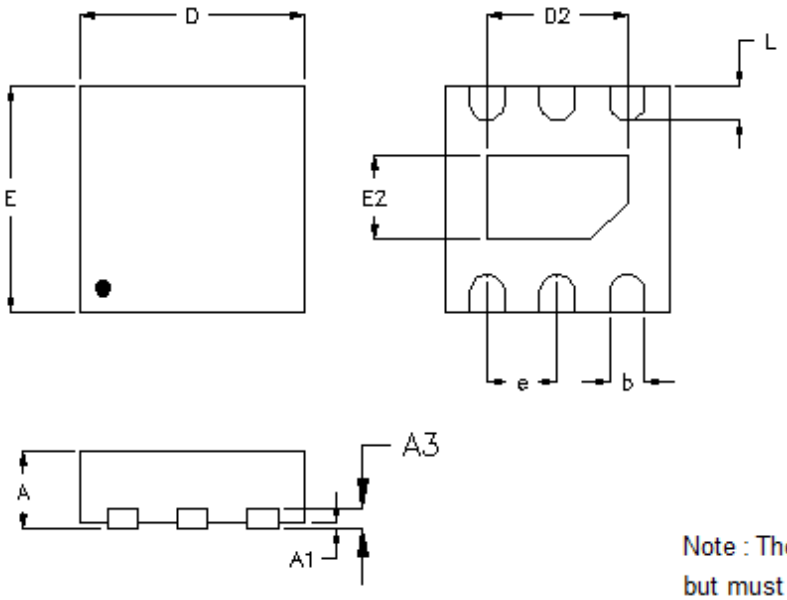
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

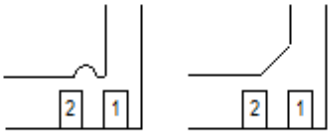
SOT-23-5 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.360	0.508	0.014	0.020
B	2.400	2.600	0.094	0.102
b1	0.406	0.533	0.016	0.021
C	3.937	4.250	0.155	0.167
C1	0.800	1.194	0.031	0.047
D	4.400	4.600	0.173	0.181
D1	1.397	1.700	0.055	0.067
e	1.400	1.600	0.055	0.063
H	0.356	0.430	0.014	0.017

5-Lead SOT-89 Surface Mount Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.175	0.004	0.007
b	0.200	0.300	0.008	0.012
D	1.500	1.700	0.059	0.067
D2	0.950	1.050	0.037	0.041
E	1.500	1.700	0.059	0.067
E2	0.550	0.650	0.022	0.026
e	0.500		0.020	
L	0.200	0.300	0.008	0.012

U-Type 6L DFN 1.6x1.6 Package

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