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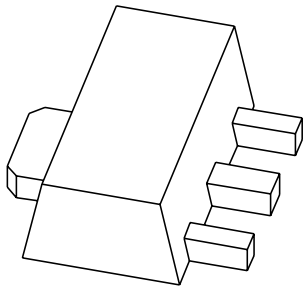
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Kind regards,

Team Nexperia

DATA SHEET



PBSS5540X

40 V, 5 A

PNP low V_{CEsat} (BISS) transistor

Product data sheet
Supersedes data of 2004 Jan 15

2004 Nov 04

40 V, 5 A PNP low V_{CEsat} (BISS) transistor

PBSS5540X

FEATURES

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- High efficiency leading to less heat generation.

APPLICATIONS

- Supply line switching circuits
- Battery management applications
- DC/DC converter applications
- Strobe flash units
- Medium power driver (e.g. relays, buzzers and motors).

DESCRIPTION

PNP low V_{CEsat} transistor in a medium power SOT89 (SC-62) package.

NPN complement: PBSS4540X.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PBSS5540X	*1G

Note

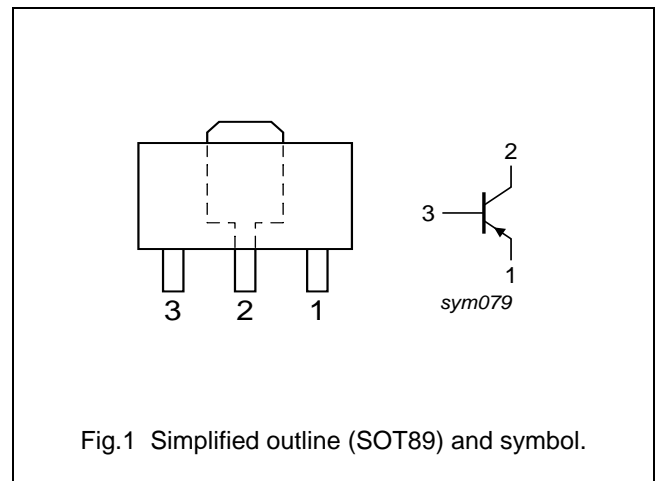
- * = p: Made in Hong Kong.
 * = t: Made in Malaysia.
 * = W: Made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	-40	V
I_C	collector current (DC)	-4	A
I_{CRP}	repetitive peak collector current	-5	A
R_{CEsat}	equivalent on-resistance	75	m Ω

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS5540X	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89

40 V, 5 A
PNP low V_{CEsat} (BISS) transistor

PBSS5540X

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

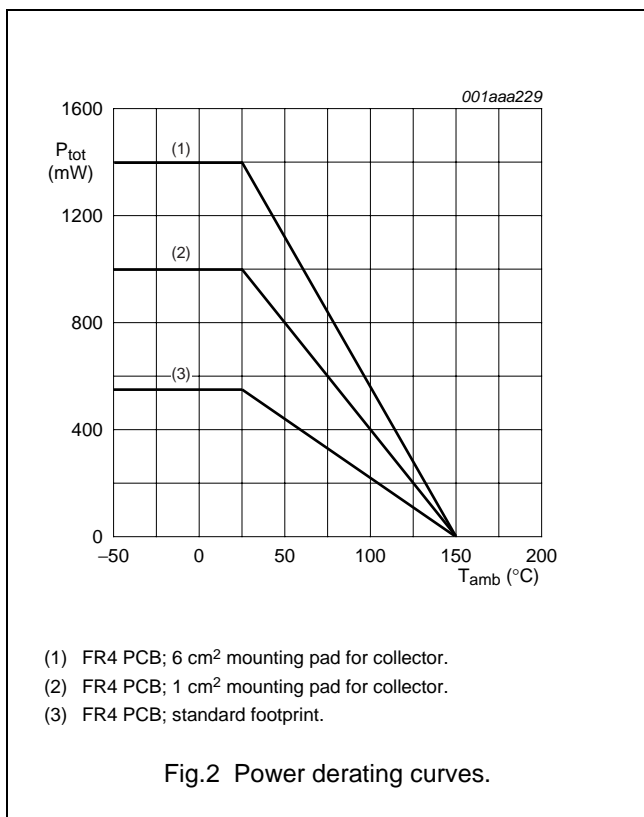
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–40	V
V_{CEO}	collector-emitter voltage	open base	–	–40	V
V_{EBO}	emitter-base voltage	open collector	–	–6	V
I_{CM}	peak collector current	$t_p \leq 1$ ms	–	–10	A
I_{CRP}	repetitive peak collector current	$t_p \leq 10$ ms; $\delta \leq 0.2$	–	–5	A
I_C	collector current (DC)		–	–4	A
I_{BM}	peak base current	$t_p \leq 1$ ms	–	–2	A
I_B	base current (DC)		–	–1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	2.5	W
		$t_p \leq 10$ ms; $\delta \leq 0.2$; note 1	–	0.55	W
		note 1	–	1	W
		note 3	–	1.4	W
		note 4	–	1.6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

Notes

1. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².
4. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated.

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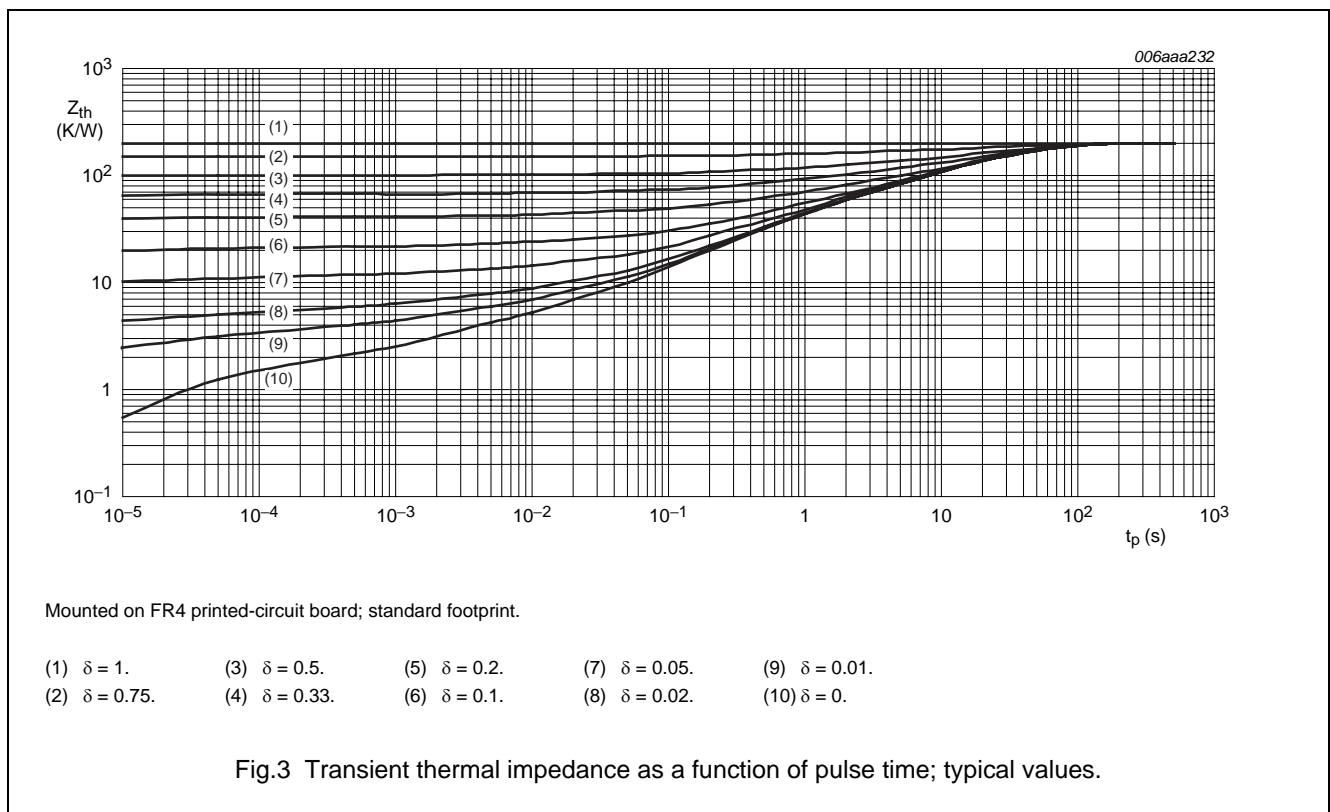
PBSS5540X

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		notes 1 and 2	50	K/W
		note 2	225	K/W
		note 3	125	K/W
		note 4	90	K/W
	note 5	80	K/W	
$R_{th(j-s)}$	thermal resistance from junction to soldering point		16	K/W

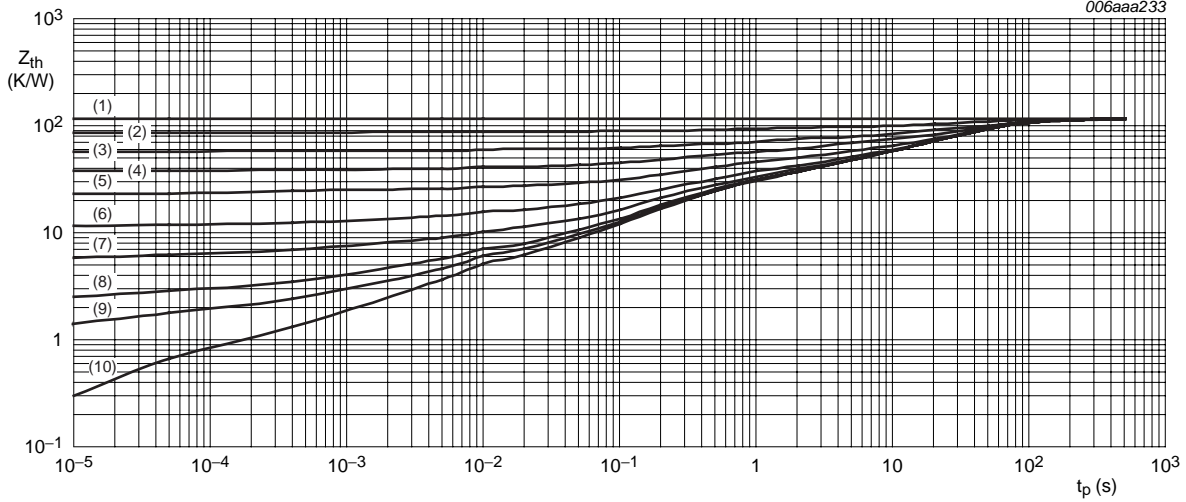
Notes

1. Pulse test: $t_p \leq 10$ ms; $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².
5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated.



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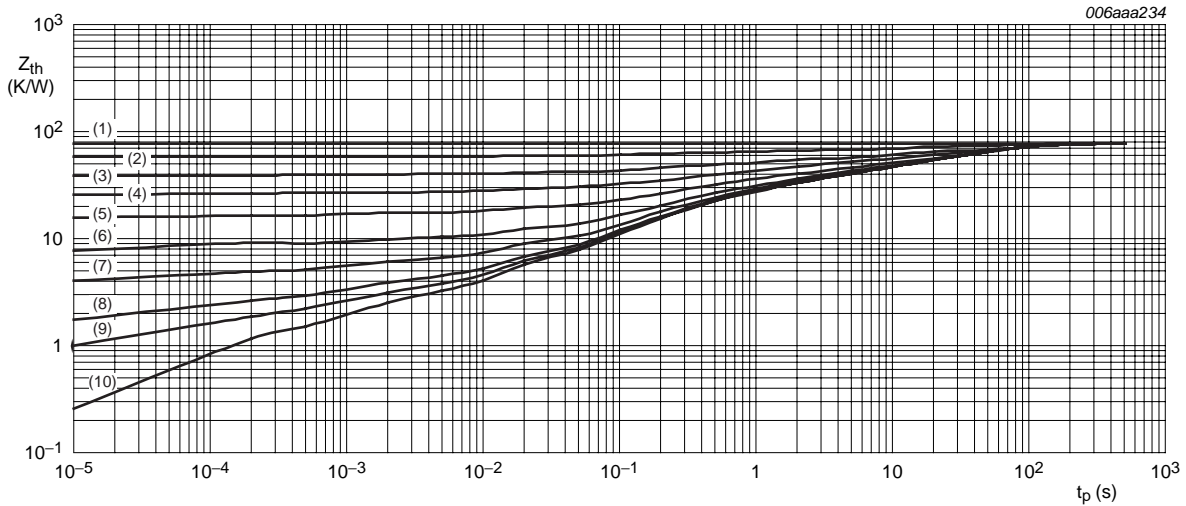
PBSS5540X



Mounted on FR4 printed-circuit board; mounting pad for collector 1 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.4 Transient thermal impedance as a function of pulse time; typical values.



Mounted on FR4 printed-circuit board; mounting pad for collector 6 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.5 Transient thermal impedance as a function of pulse time; typical values.

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CHARACTERISTICS $T_{amb} = 25\text{ °C}$ unless otherwise specified.

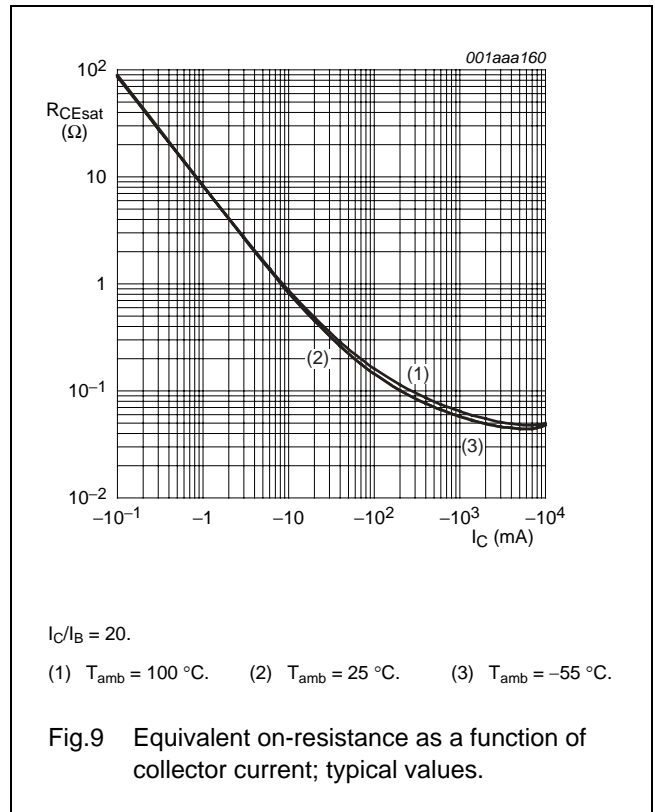
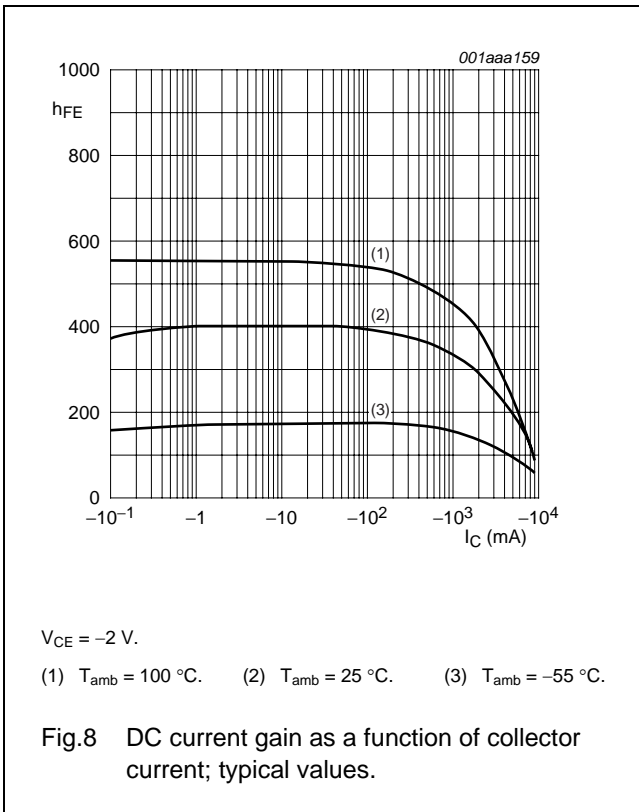
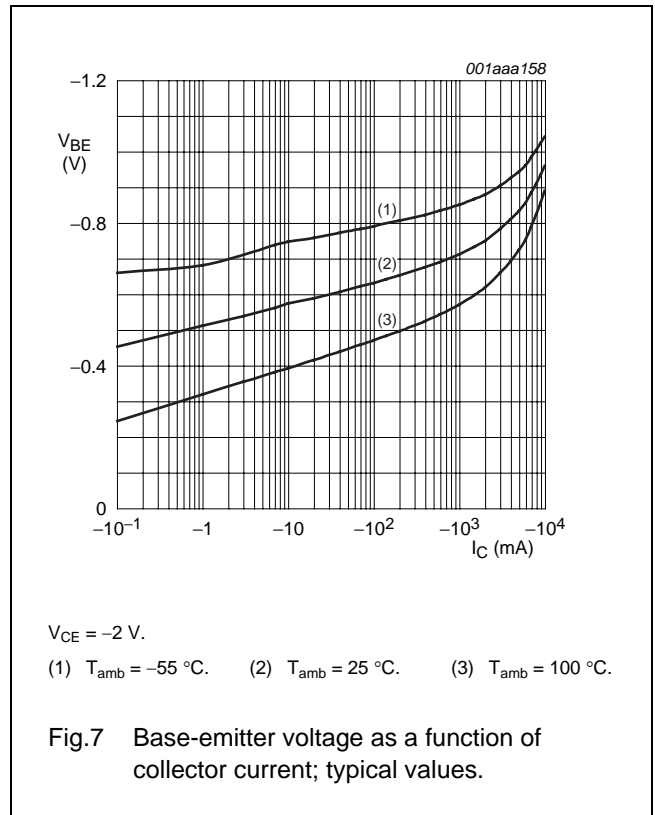
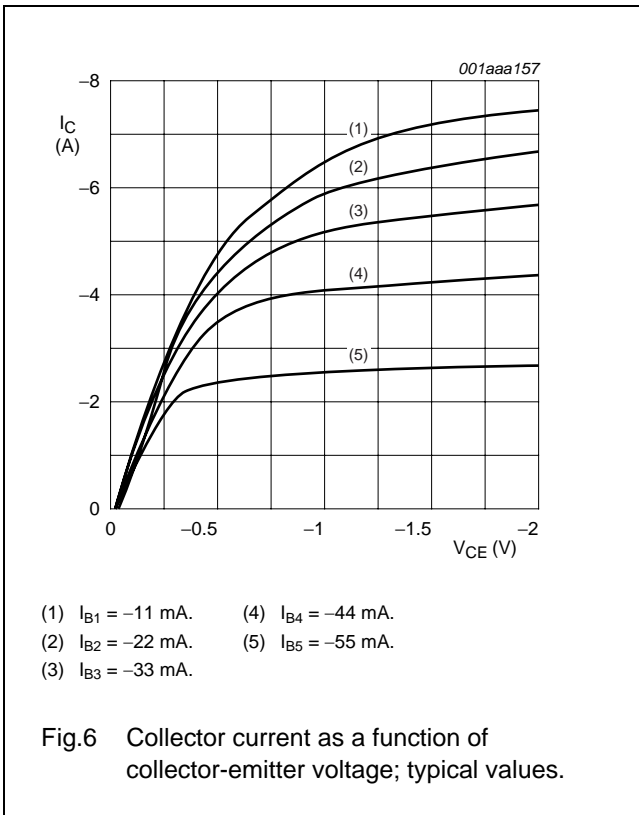
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0\text{ A}$	–	–	–100	nA
		$V_{CB} = -30\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ °C}$	–	–	–50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	–	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}; I_C = -0.5\text{ A}$	250	–	–	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A};$ note 1	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A};$ note 1	150	–	–	
		$V_{CE} = -2\text{ V}; I_C = -5\text{ A};$ note 1	50	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -5\text{ mA}$	–	–	120	mV
		$I_C = -1\text{ A}; I_B = -10\text{ mA}$	–	–	170	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–	160	mV
		$I_C = -4\text{ A}; I_B = -200\text{ mA};$ note 1	–	–	340	mV
		$I_C = -5\text{ A}; I_B = -500\text{ mA};$ note 1	–	–	375	mV
R_{CEsat}	equivalent on-resistance	$I_C = -5\text{ A}; I_B = -500\text{ mA};$ note 1	–	45	75	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -4\text{ A}; I_B = -200\text{ mA};$ note 1	–	–	–1.1	V
		$I_C = -5\text{ A}; I_B = -500\text{ mA};$ note 1	–	–	–1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	–	–	–1.0	V
f_T	transition frequency	$V_{CE} = -10\text{ V}; I_C = -0.1\text{ A};$ $f = 100\text{ MHz}$	60	–	–	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_E = 0\text{ A};$ $f = 1\text{ MHz}$	–	–	105	pF

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

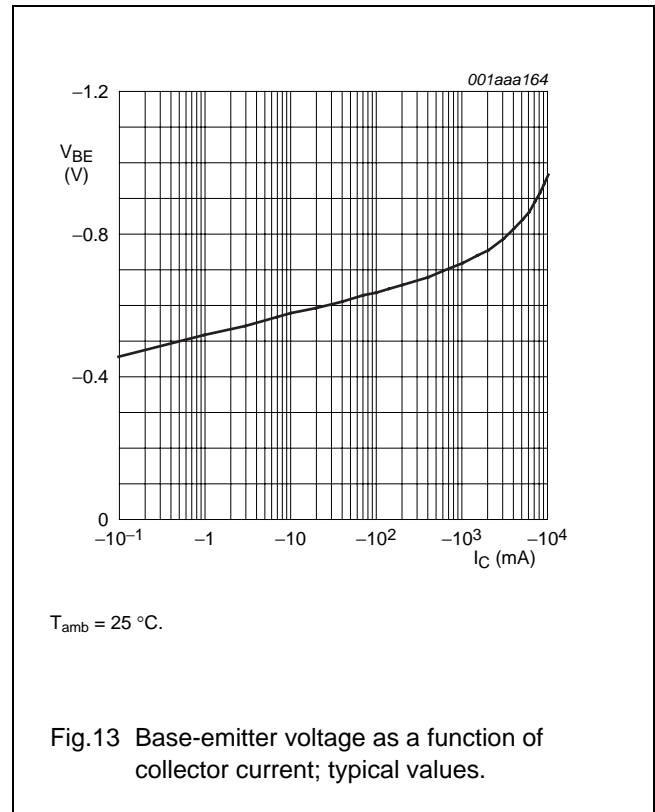
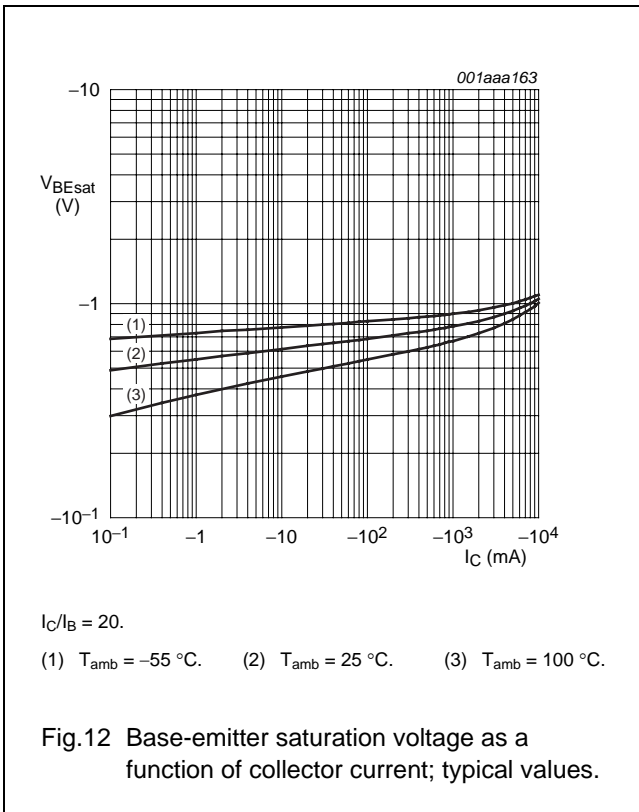
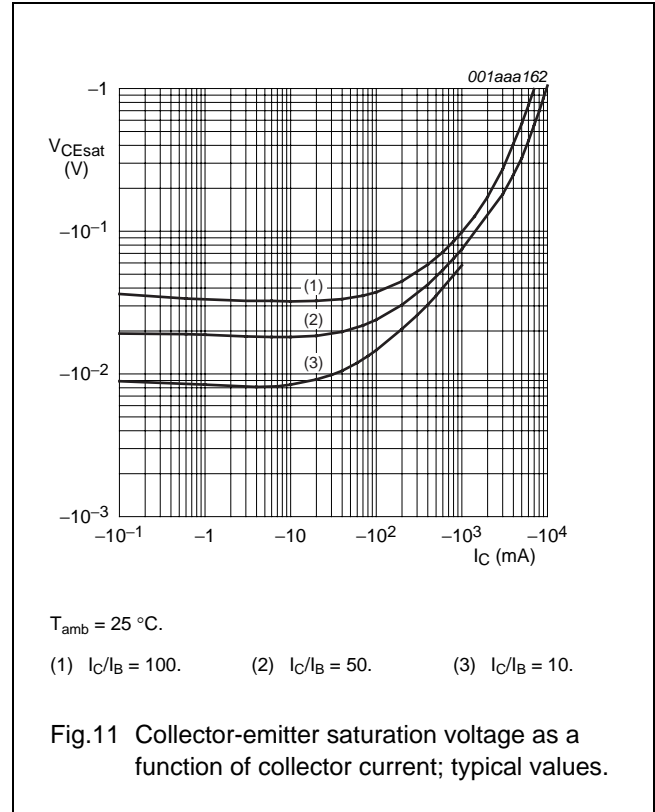
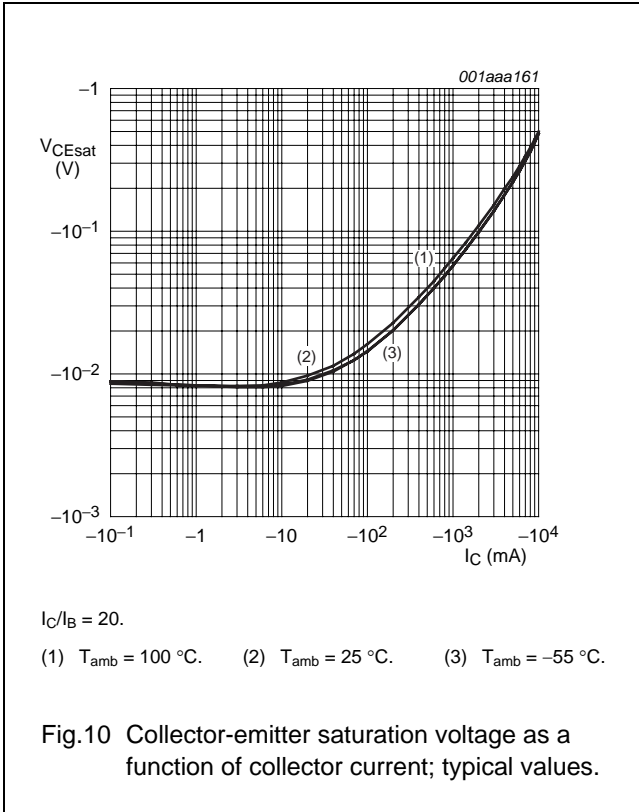
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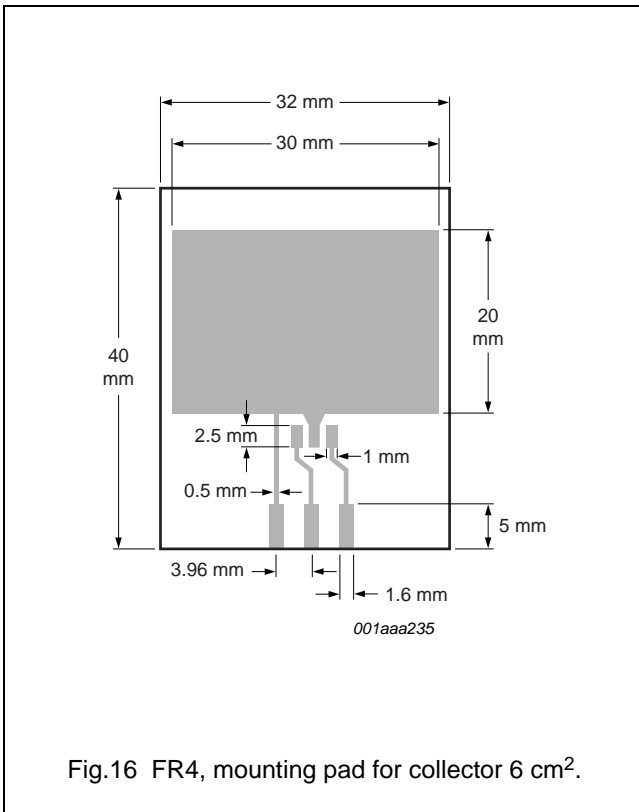
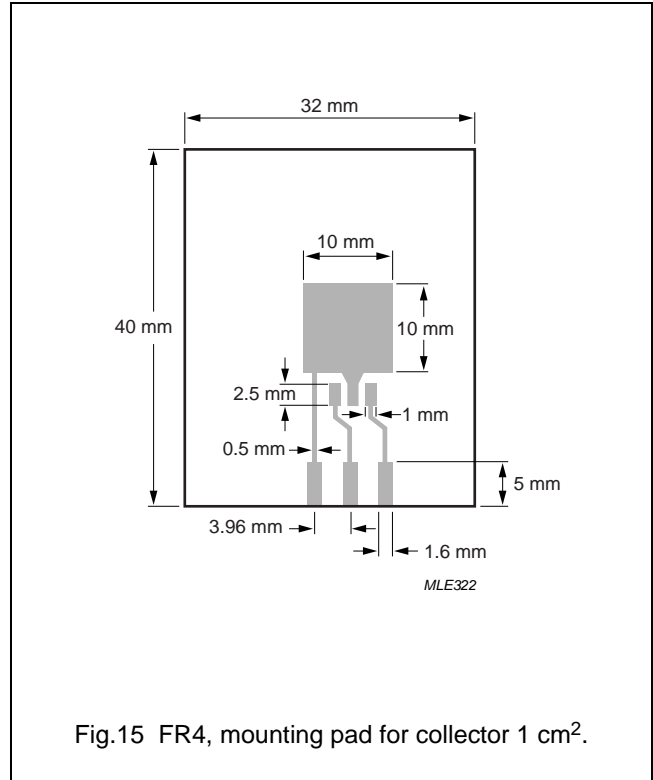
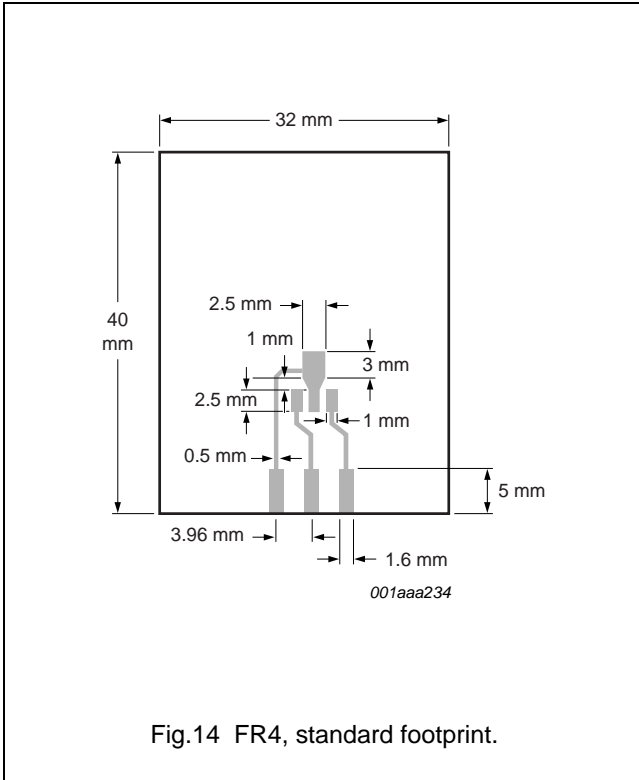
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Reference mounting conditions



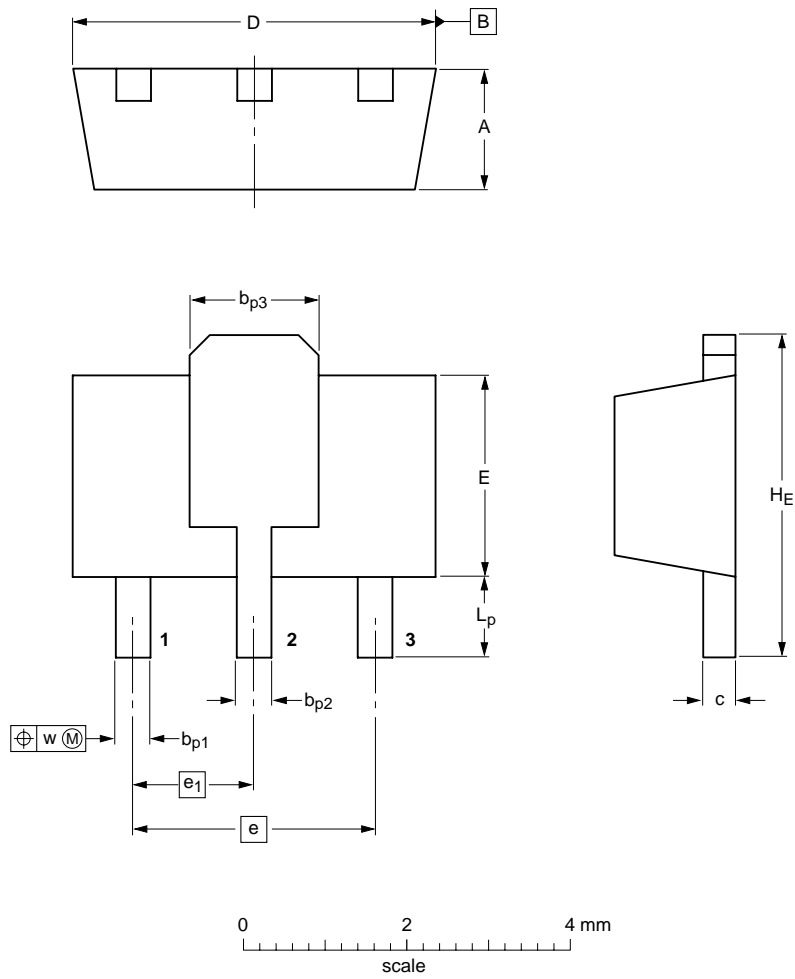
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PACKAGE OUTLINE

Plastic surface-mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_{p1}	b_{p2}	b_{p3}	c	D	E	e	e_1	H_E	L_p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT89		TO-243	SC-62		04-08-03 06-03-16

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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NXP Semiconductors

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