NTGD3133P

Power MOSFET
−20 V, −2.5 A, P−Channel, TSOP−6 Dual

Features

- Reduced Gate Charge for Fast Switching
- −2.5 V Gate Rating
- Leading Edge Trench Technology for Low On Resistance
- Independent Devices to Provide Design Flexibility
- This is a Pb−Free Device

Applications

- Li−Ion Battery Charging
- Load Switch / Power Switching
- DC to DC Conversion
- Portable Devices like PDA's, Cellular Phones, and Hard Drives

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−20	V
Gate−to−Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−2.2	A
		T_A = 85°C		−1.6	
	t ≤ 5 s	T_A = 25°C		−2.5	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.0	W
	t ≤ 5 s			1.3	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−1.6	A
		T_A = 85°C		−1.2	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.56	W
Pulsed Drain Current		t_p = 10 μs	I_{DM}	−7.5	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	−0.8	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

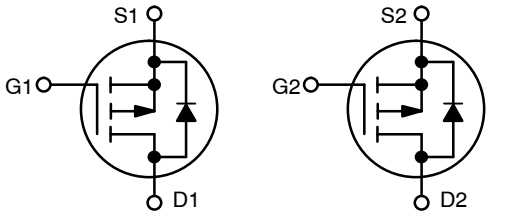
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 30 mm^2 [2 oz] including traces).

ON Semiconductor®

http://onsemi.com

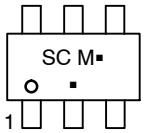
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−20 V	145 mΩ @ −4.5 V	−2.2 A
	200 mΩ @ −2.5 V	−1.6 A



P−CHANNEL MOSFET **P−CHANNEL MOSFET**

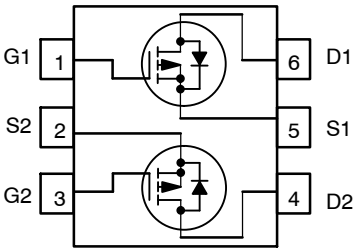
TSOP6
CASE 318G
STYLE 13

MARKING DIAGRAM



SC = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTGD3133PT1G	TSOP6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2008

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	115	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 3)	$R_{\theta JA}$	95	
Junction−to−Ambient − Steady State Min Pad (Note 4)	$R_{\theta JA}$	225	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 30 mm^2 [2 oz] including traces).

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	I_D = −250 μA	−20	−	−	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			−	14.2	−	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −16 V	T_J = 25°C	−	−	−1.0	μA
			T_J = 85°C	−	−	−10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V		−	−	±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}	I_D = −250 μA	−0.6	−0.95	−1.4	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −2.2 A		−	90	145	mΩ
		V_{GS} = −2.5 V, I_D = −1.6 A		−	140	200	
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V, I_D = −2.2 A		−	4.5	−	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = −10 V, f = 1.0 MHz		−	400	−	pF
Output Capacitance	C_{OSS}			−	75	−	
Reverse Transfer Capacitance	C_{RSS}			−	40	−	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −2.2 A		−	3.8	5.5	nC
Threshold Gate Charge	$Q_{G(TH)}$			−	0.5	−	
Gate−to−Source Charge	Q_{GS}			−	0.9	−	
Gate−to−Drain Charge	Q_{GD}			−	1.0	−	
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −1.0 A, R_G = 6.0 Ω		−	6.7	−	ns
Rise Time	t_r			−	12.7	−	
Turn−Off Delay Time	$t_{d(OFF)}$			−	13.2	−	
Fall Time	t_f			−	11	−	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, T_J = 25°C	I_S = −0.8 A	−	−0.8	−1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_{SD} / dt = 100 A/μs, I_S = −0.8 A		−	12	−	ns
Charge Time	t_a			−	8.0	−	
Discharge Time	t_b			−	4.0	−	
Reverse Recovery Charge	Q_{RR}			−	4.0	−	nC

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CHARACTERISTICS

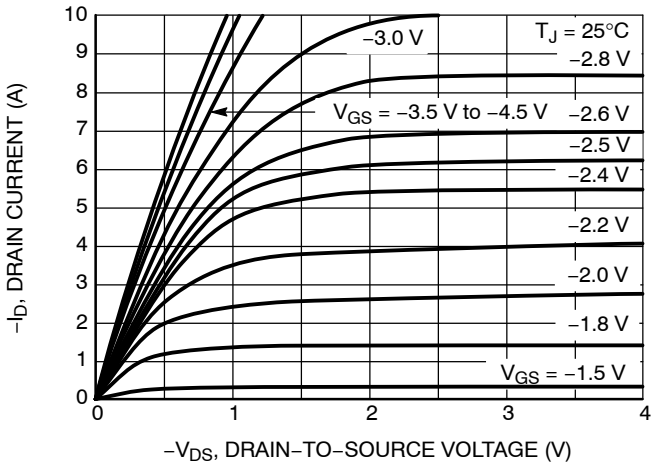


Figure 1. On−Region Characteristics

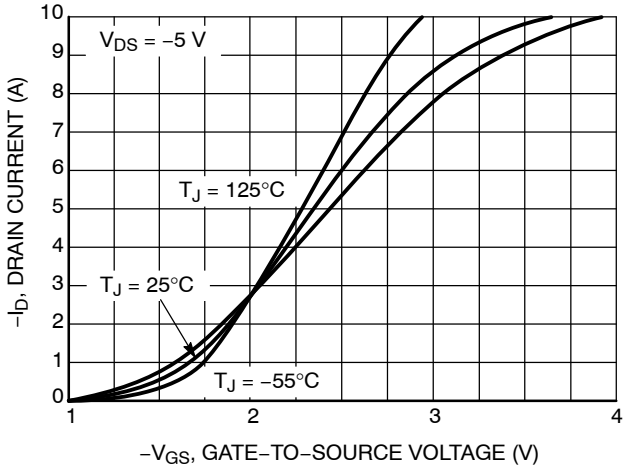


Figure 2. Transfer Characteristics

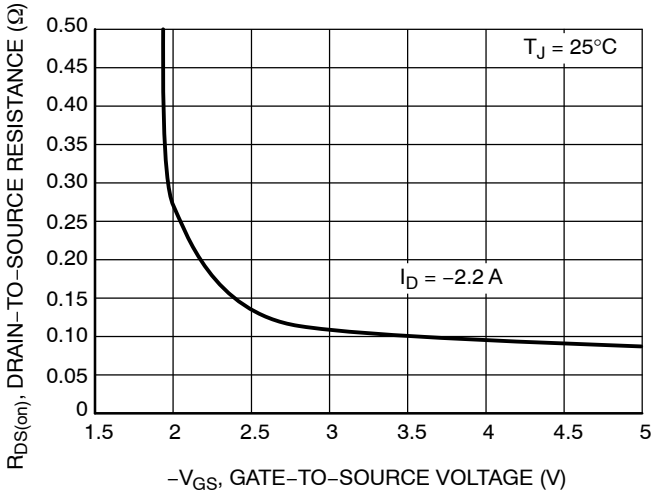


Figure 3. On−Resistance versus Gate−to−Source Voltage

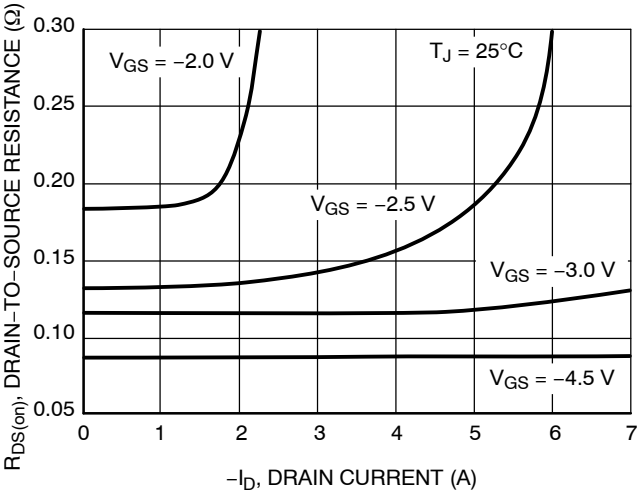


Figure 4. On−Resistance versus Drain Current and Gate Voltage

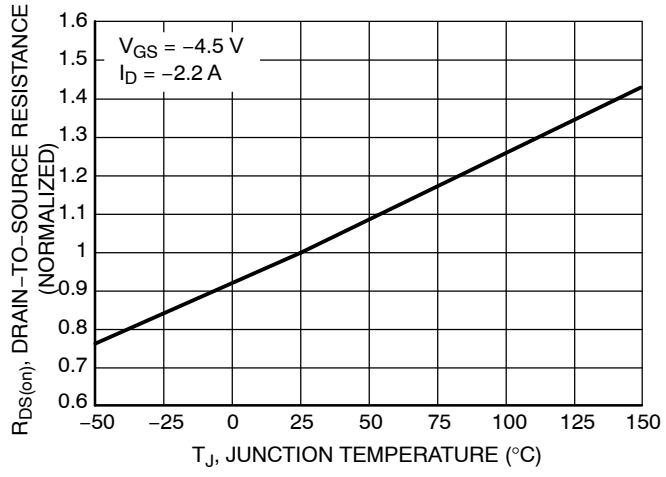


Figure 5. On−Resistance Variation with Temperature

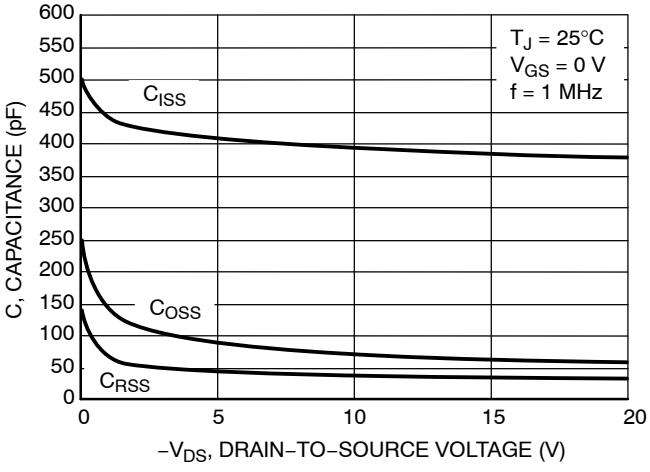


Figure 6. Capacitance Variation

TYPICAL PERFORMANCE CHARACTERISTICS

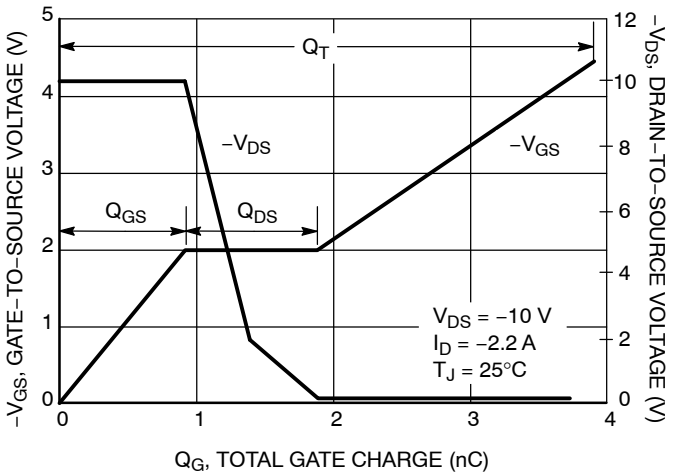


Figure 7. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

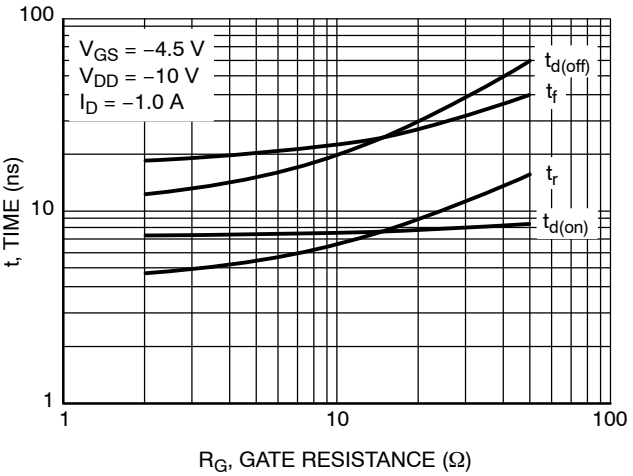


Figure 8. Resistive Switching Time Variation versus Gate Resistance

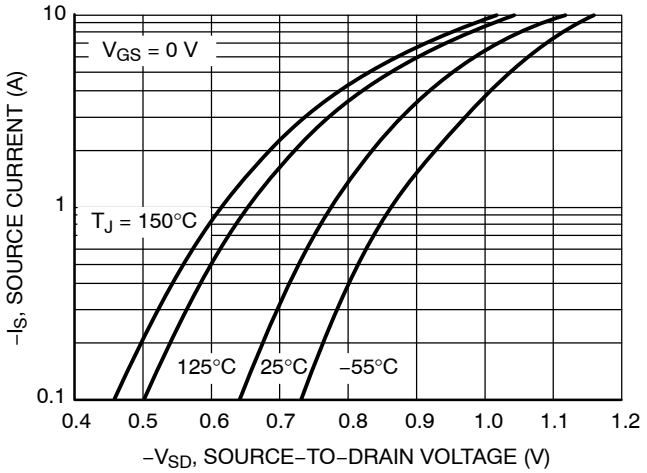


Figure 9. Diode Forward Voltage versus Current

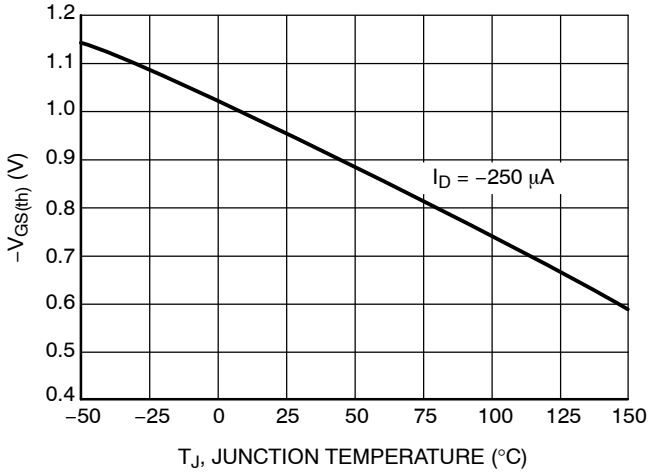


Figure 10. Threshold Voltage

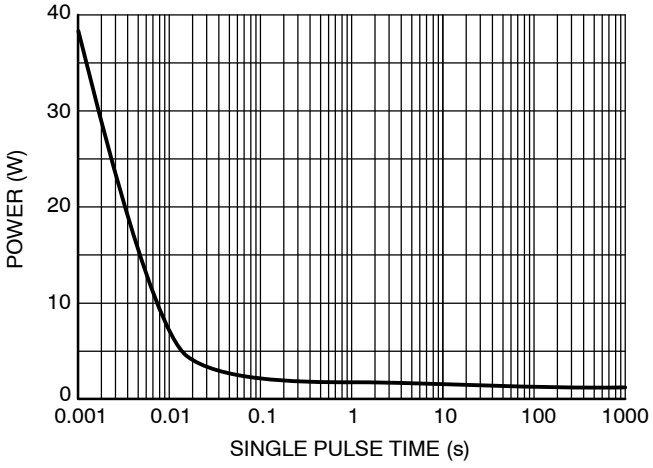


Figure 11. Single Pulse Maximum Power Dissipation

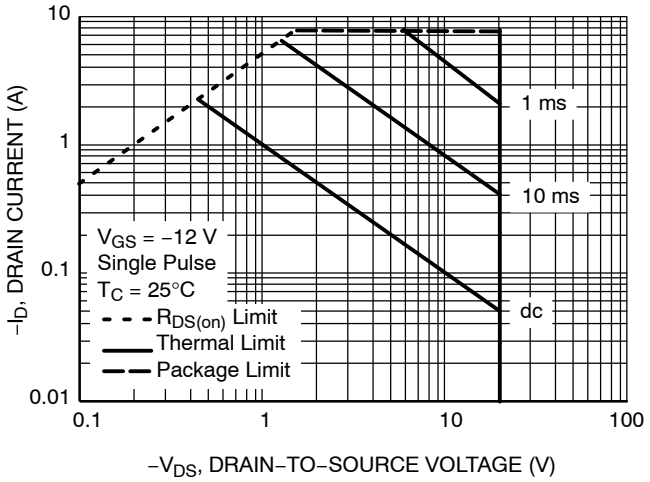


Figure 12. Maximum Rated Forward Biased Safe Operating Area

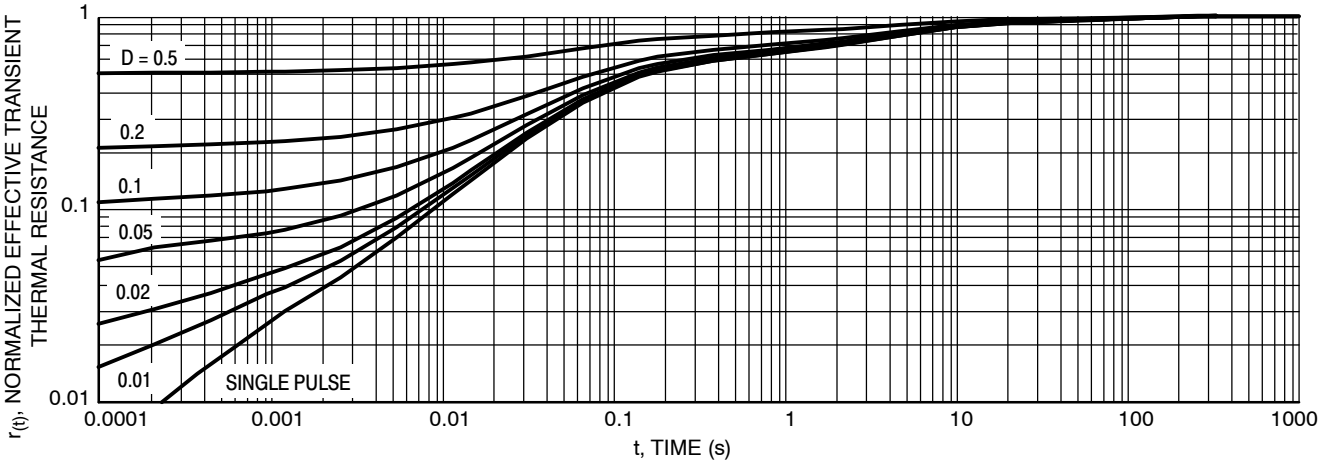
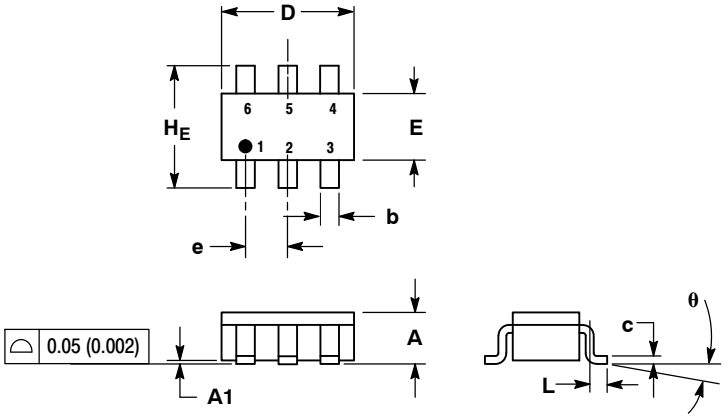


Figure 13. Thermal Response

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE S

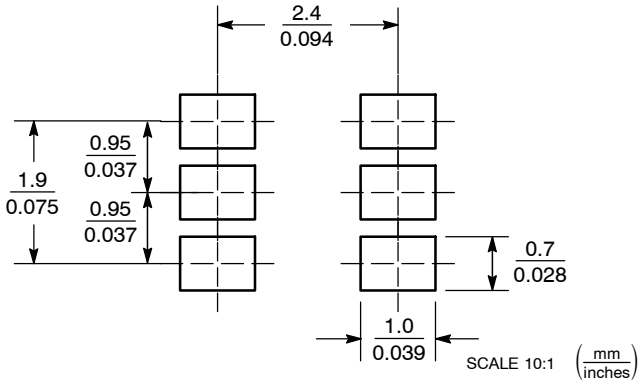


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NTGD3133P/D