MP6533

5V to 60V, Three-Phase Brushless DC Motor Pre-Driver

The Future of Analog IC Technology

DESCRIPTION

The MP6533 is a gate driver IC designed for three-phase brushless DC motor driver applications. It is capable of driving three half bridges consisting of six N-channel power MOSFETs up to 60V.

The MP6533 uses a bootstrap capacitor to generate a supply voltage for the high-side MOSFET driver. An internal trickle-charge circuit maintains sufficient gate driver voltage at 100% duty cycle.

Internal safety features include programmable over-current protection, a motor start-up current limit, adjustable dead-time control, UVLO, and thermal shutdown.

The device has three Hall-element inputs. Commutation logic is determined by three Hall-element inputs spaced at 120°. The PWM, DIR, and nBRAKE inputs are used to control motor speed, direction, and brake engagement.

The MP6533 is available in a 28-pin 9.7mm x 6.4mm TSSOP with an exposed thermal pad.

FEATURES

- Wide 5V to 60V Input Voltage Range
- Hall Signal Interface
- Bootstrap Gate Driver with Trickle-Charge Circuit Supports 100% Duty Cycle Operation
- Low-Power Sleep Mode for Battery-Powered Applications
- Programmable Over-Current Protection of External MOSFETs
- Adjustable Dead-Time Control to Prevent Shoot-Through
- PWM Speed-Control Input
- Brake Input
- Motor Start-Up Current Limit
- Thermal Shutdown and UVLO Protection
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package

APPLICATIONS

- Three-Phase Brushless DC Motors and Permanent Magnet Synchronous Motors
- Power Drills
- Impact Drivers
- E-Bike

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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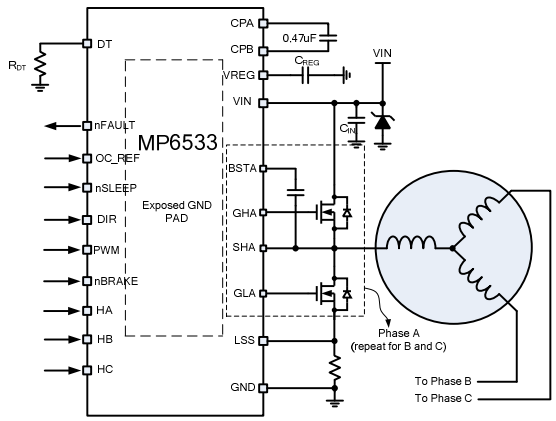
TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6533GF	TSSOP-28 EP	*See Below*

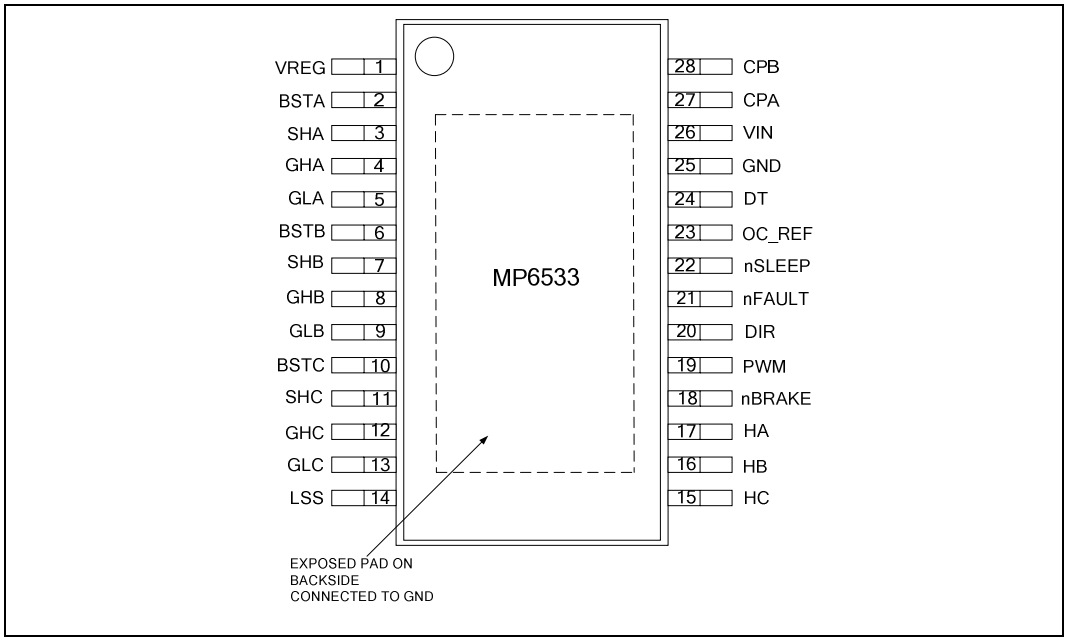
* For Tape & Reel, add suffix –Z (e.g. MP6533GF–Z);

TOP MARKING

MPSYYWW
MP6533
LLLLLLLLL

MPS: MPS prefix:
YY: year code;
WW: week code:
MP6533: part number;
LLLLLLLLL: lot number;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{IN} ..... -0.3V to 65V
CPA ..... -0.3V to 60V
CPB ..... -0.3V to 12.5V
VREG ..... -0.3V to 13V
BSTA/B/C ..... -0.3V to 70V
GHA/B/C ..... -0.3V to 70V
SHA/B/C ..... -0.3V to 65V
GLA/B/C ..... -0.3V to 13V
LSS ..... -0.3V to 1V
All Other Pins to AGND ..... -0.3V to 6.5V
Continuous Power Dissipation (T_A = +25°C) **(2)**
TSSOP-28 EP 3.9W
Storage Temperature ..... -55°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Solder) ..... +260°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... 5V to 60V
OC_REF Voltage V_{OC} .....0.125V to 2.4V
Operating Junct. Temp (T_J)..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSSOP-28 EP	32	6	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input Supply Voltage	V_{IN}		5		60	V
Quiescent Current	I_Q	nSLEEP=1, gate not switching		0.95	2	mA
	I_{SLEEP}	nSLEEP=0			1	µA
Control Logic						
Input Logic 'Low' Threshold	V_{IL}				0.8	V
Input Logic 'High' Threshold	V_{IH}		2			V
Logic Input Current	$I_{IN(H)}$	V_{IH}=5V	-20		20	µA
	$I_{IN(L)}$	V_{IL}=0.8V	-20		20	µA
nSLEEP Pull Down Current	$I_{SLEEP-PD}$			1		µA
Internal Pull Down Resistance	R_{PD}			880		kΩ
Fault Outputs(Open-Drain Outputs)						
Output Low Voltage	V_{OL}	I_O=5mA			0.5	V
Output High Leakage Current	I_{OH}	V_O=3.3V			1	µA
Protection Circuit						
UVLO Rising Threshold	V_{IN_RISE}		3.3	3.9	4.5	V
UVLO Hysteresis	V_{IN_HYS}			200		mV
VREG Rising Threshold	V_{REG_RISE}		6.8	7.6	8.4	V
VREG Hysteresis	V_{REG_HYS}			0.54	1	V
VREG Startup Delay	t_{REG}			700		µs
OC_REF Threshold	V_{OC}	V_{OC}=1V, T_J =25°C	0.8	1	1.2	V
		V_{OC}=2.4V, T_J =25°C	2.18	2.4	2.62	V
OCP Deglitch Time	t_{OC}			3		µs
SLEEP Wakeup Time	t_{SLEEP}			1		ms
LSS Current Limit Threshold	V_{LSS}		0.4	0.5	0.6	V
LSS Current Limit Fixed Off Time	t_{OFF}		53	66	80	us
LSS Current Limit High side Minimum On Time	t_{ON}			1		us
Thermal Shutdown	T_{TSD}			150		°C

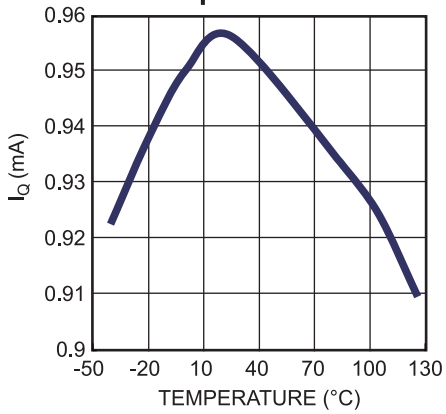
ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

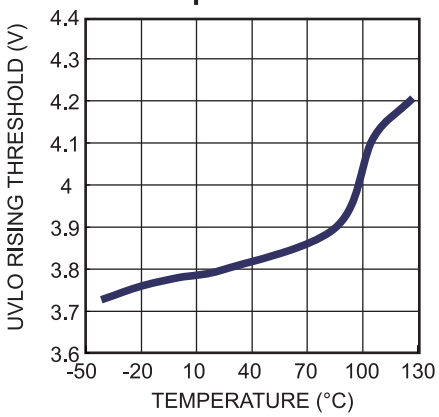
Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate Drive						
Bootstrap Diode Forward Voltage	V_{FBOOT}	I_D=10mA			0.9	V
		I_D=100mA			1.3	V
VREG Output Voltage	V_{REG}	V_{IN}=5.5V-60V T_J =25°C	10	11.5	12.8	
		V_{IN}=5V	2xV_{IN}-1			V
Gate Drive Pull Up Resistance	R_{UP}	V_{DS}=1V		8		Ω
HS Gate Drive Pull Down Resistance	R_{HS-DN}	V_{DS}=1V	1.2		4.3	Ω
LS Gate Drive Pull Down Resistance	R_{LS-DN}	V_{DS}=1V	1		5	Ω
LS Passive Pull Down Resistance	R_{LS-PDN}			590		kΩ
LS Automatic Turn On Time	t_{LS}			1.8		µs
Charge Pump Frequency	f_{CP}			110		kHz
Dead Time	t_{DEAD}	Leave DT Open		6		µs
		R_{DT}=200kΩ		0.74		µs
		DT tied to GND		30		ns

TYPICAL CHARACTERISTICS

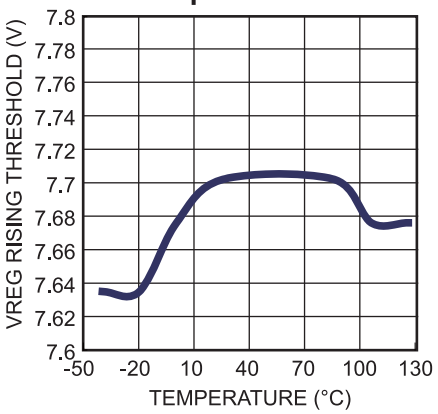
Quiescent Current vs. Temperature



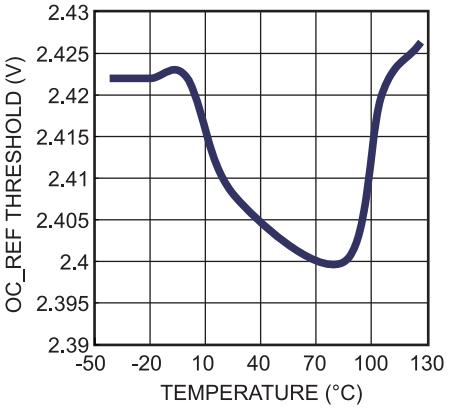
UVLO Rising Threshold vs. Temperature



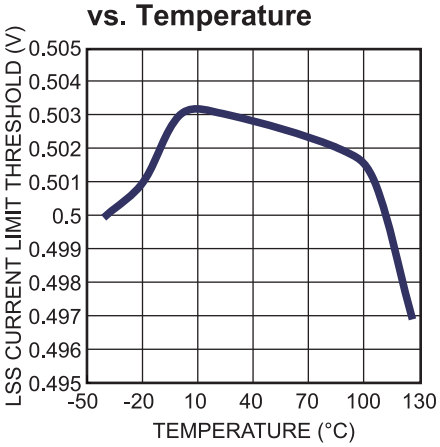
VREG Rising Threshold vs. Temperature



OC_REF Threshold vs. Temperature



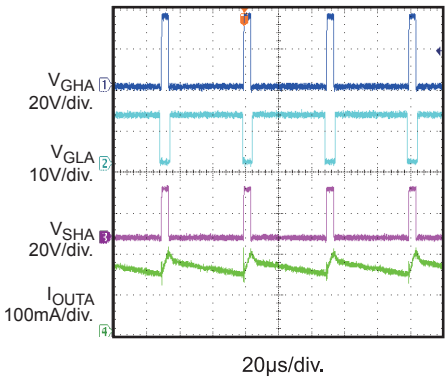
LSS Current Limit Threshold vs. Temperature



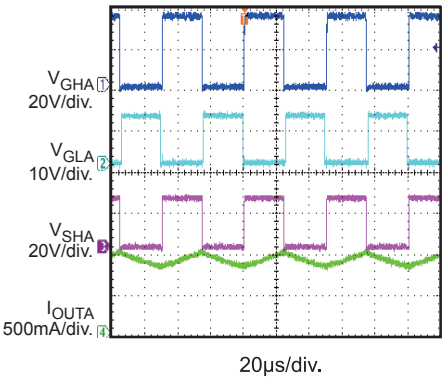
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=24V, OC_REF=0.5V, R_{DT}=200k, DIR=H, HA=HC=H, HB=L, F_{PWM}=20kHz, T_A=25°C, Resistor+Inductor Load: 5ohm+1mH/phase with star connection, unless otherwise noted.

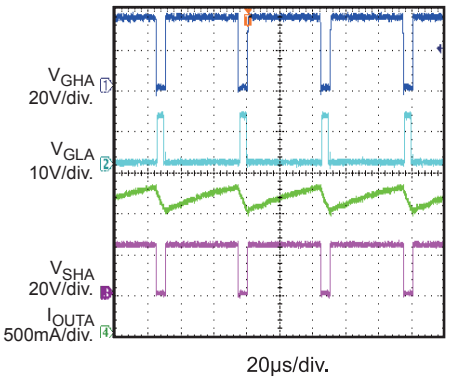
Steady State
Duty=10%



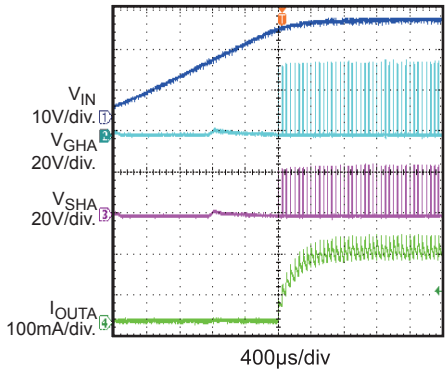
Steady State
Duty=50%



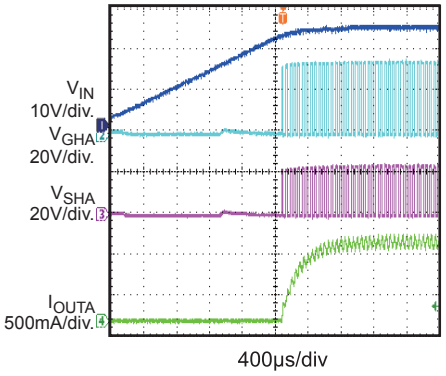
Steady State
Duty=90%



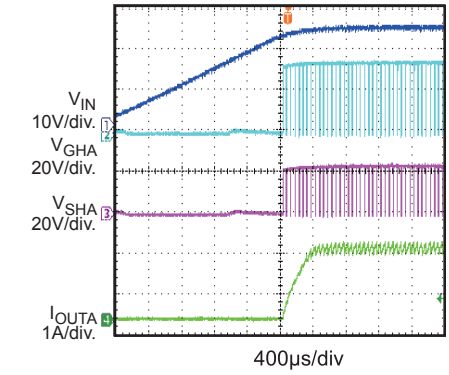
Power Ramp Up
Duty=10%



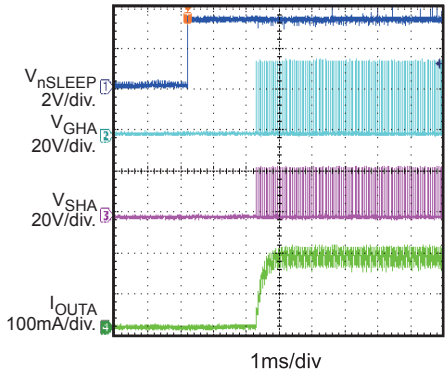
Power Ramp Up
Duty=50%



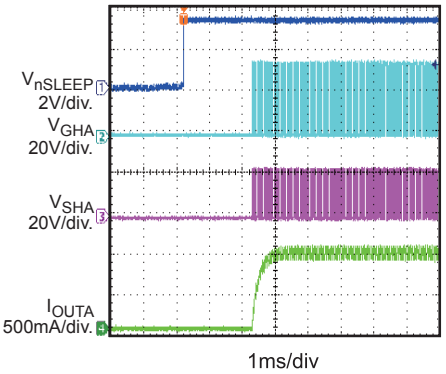
Power Ramp Up
Duty=90%



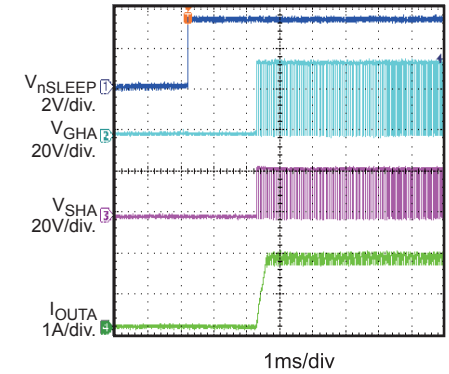
Sleep Recovery
Duty=10%



Sleep Recovery
Duty=50%



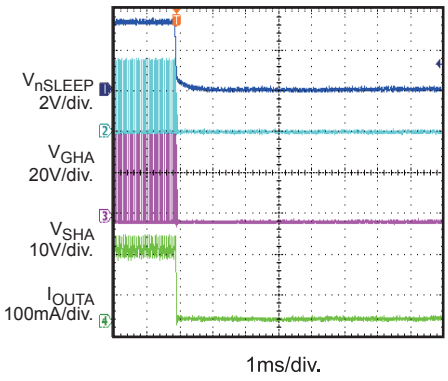
Sleep Recovery
Duty=90%



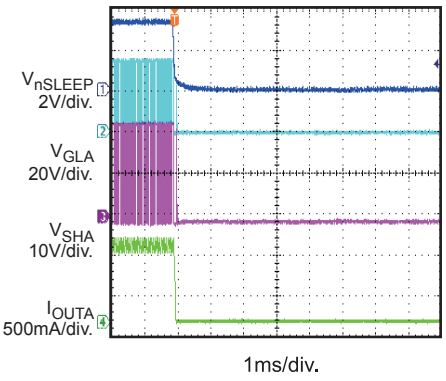
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=24V, OC_REF=0.5V, R_{DT}=200k, DIR=H, HA=HC=H, HB=L, F_{PWM}=20kHz, T_A=25°C, Resistor+Inductor Load: 5ohm+1mH/phase with star connection, unless otherwise noted.

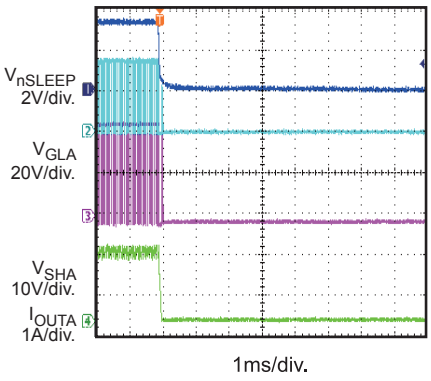
Sleep Entry
Duty=10%



Sleep Entry
Duty=50%



Sleep Entry
Duty=90%



PIN FUNCTIONS

Pin #	Name	Description
1	VREG	**Gate drive supply output.**
2	BSTA	**Bootstrap output phase A.**
3	SHA	**High-side source connection phase A.**
4	GHA	**High-side gate drive phase A.**
5	GLA	**Low-side gate drive phase A.**
6	BSTB	**Bootstrap output phase B.**
7	SHB	**High-side source connection phase B.**
8	GHB	**High-side gate drive phase B.**
9	GLB	**Low-side gate drive phase B.**
10	BSTC	**Bootstrap output phase C.**
11	SHC	**High-side source connection phase C.**
12	GHC	**High-side gate drive phase C.**
13	GLC	**Low-side gate drive phase C.**
14	LSS	**Low-side source connection.**
15	HC	**Hall-sensor input, phase C.**
16	HB	**Hall-sensor input, phase B.**
17	HA	**Hall-sensor input, phase A.**
18	nBRAKE	**An active-low logic input for a braking function.**
19	PWM	**External PWM control for speed/torque.**
20	DIR	**A logic input to determine the direction of motor torque output.**
21	nFAULT	**Fault indication.** Open-drain output. nFAULT is logic low when in a fault condition.
22	nSLEEP	**Sleep mode input.** Logic low to enter low-power sleep mode. Float to enable.
23	OC_REF	**Over-current protection reference input.**
24	DT	**Dead time setting.**
25	GND	**Ground.**
26	VIN	**Input supply voltage.**
27	CPA	**Charge pump capacitor connect terminal.**
28	CPB	**Charge pump capacitor connect terminal.**

BLOCK DIAGRAM

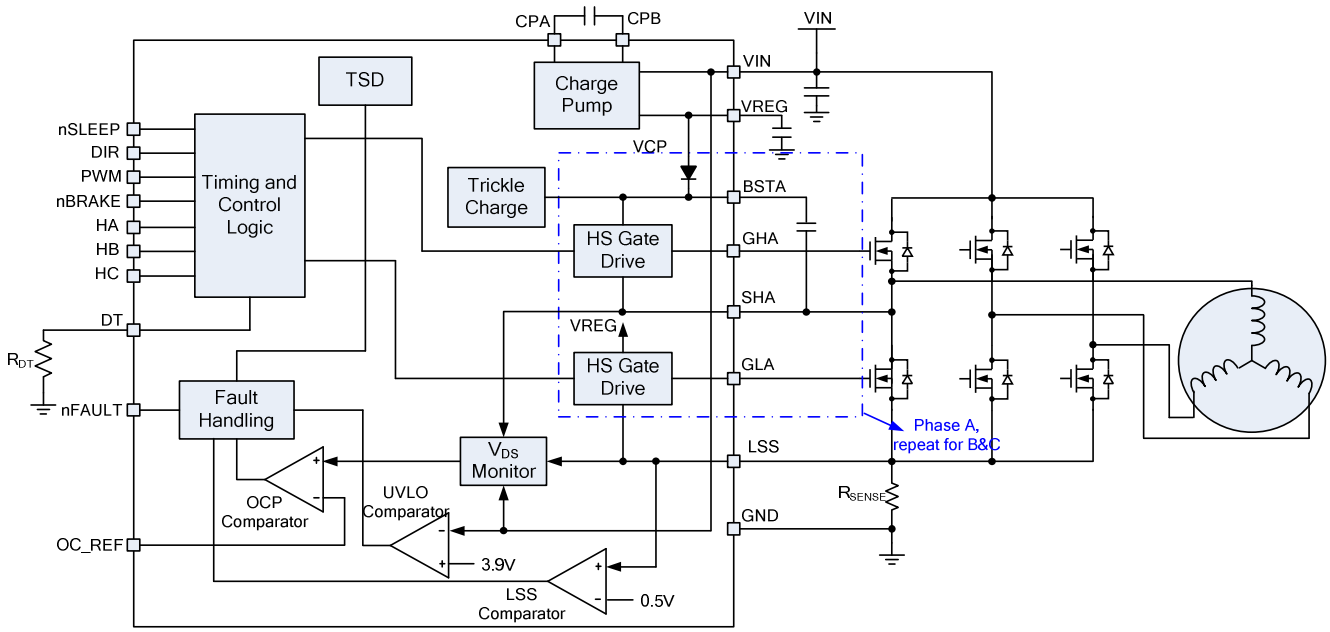


Figure 1: Functional Block Diagram

OPERATION

The MP6533 is a three-phase BLDC motor pre-driver that can drive three half bridges with a 0.8A source and a 1A sink current capability over a wide input voltage range of 5V to 60V. It is designed for use in battery-powered equipment. The MP6533 features a low-power sleep mode, which disables the device and draws a very low supply current.

The MP6533 provides several flexible functions, such as adjustable dead-time control and over-current protection, which allow the device to cover a wide range of application fields.

nFAULT

nFAULT reports to the system when a fault condition (such as OCP and OTP) is detected. nFAUlt can be an open-drain output, and it is driven low once a fault condition occurs. If the fault condition is released, nFAULT is pulled high by an external pull-up resistor.

Over-Current Protection

To protect the power stage from damage due to high currents, a VDS sensing circuitry is implemented in the MP6533. Based on R_{DS-ON} of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated which triggers the OC protection feature when exceeded. This voltage threshold level is programmable through the OC_REF terminal by applying an external reference voltage with a DAC. Once an OCP event is detected, MP6533 will enter a latched fault state and disable all functions. MP6533 will stay latched off until it is reset by nSLEEP or UVLO.

Motor Startup Current Limit

MP6533 limits the motor startup current by monitoring the voltage at LSS pin. When the voltage at LSS exceeds the current limit threshold of 0.5V, the high side will turn off and the corresponding low side turns on for a fixed off time. After the fixed off time, the high side will turn back on and the cycle repeats until LSS no longer exceeds the current limit threshold. The current limit level is selected by the value of the current sense resistor at LSS pin.

OCP Deglitch Time

Usually, there is a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously triggering OCP and shutting down the external MOSFET. An internal fixed deglitch time (t_{OC}) blanks the output of the VDS monitor when the outputs are switched (which is also the minimum on time for the MOSFET).

Dead Time Adjustment

To prevent shoot-through in any phase of the bridge, it is necessary to have a dead time (t_{DEAD}) between a high- or low-side turn-off and the next complementary turn-on event. The dead time for all three phases is set by a single dead-time resistor (R_{DT}) between DT and ground with Equation(1):

$$t_{DEAD}(nS) = 3.7*R(k\Omega) \quad (1)$$

If DT is tied to GND directly, an internal minimum dead time (30ns) will be applied. Leaving DT open generates a 6µs dead time.

Input UVLO Protection

If at any time the voltage on VIN falls below the under-voltage lockout threshold voltage, all circuitry in the device is disabled and the internal logic will be reset. Operation will resume when VIN rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, the MP6533 enters a latched fault state similar to an OCP event, and nFAULT is driven low. Only resetting by nSLEEP or UVLO will unlatch the device from an OTP fault lockout.

Input Logic

Driving nSLEEP low will put the device into a low-power sleep state. In this state, all the internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When exiting sleep mode, a brief time period (approximately 1ms) must pass before issuing a PWM command. This time period allows the internal circuitry to stabilize.

The commutation logic is determined by three Hall-element inputs spaced at 120°. The PWM, DIR, and nBRAKE inputs are used to control motor speed/torque, direction, and to engage brake to stop the motor.

Refer to Table 1 for the logic truth table and Table 2 for the commutation Table with nBRAKE=1. If nBRAKE=0, the braking function would be active, all low-side gates on.

Table 1: Input Logic Truth Table

PWM	nBRAKE	Mode of Operation
0	1	PWM chop mode, and the load current decays
0	0	Brake mode – All low-side gates on
1	1	Selected drivers on
1	0	Brake mode – All low-side gates on

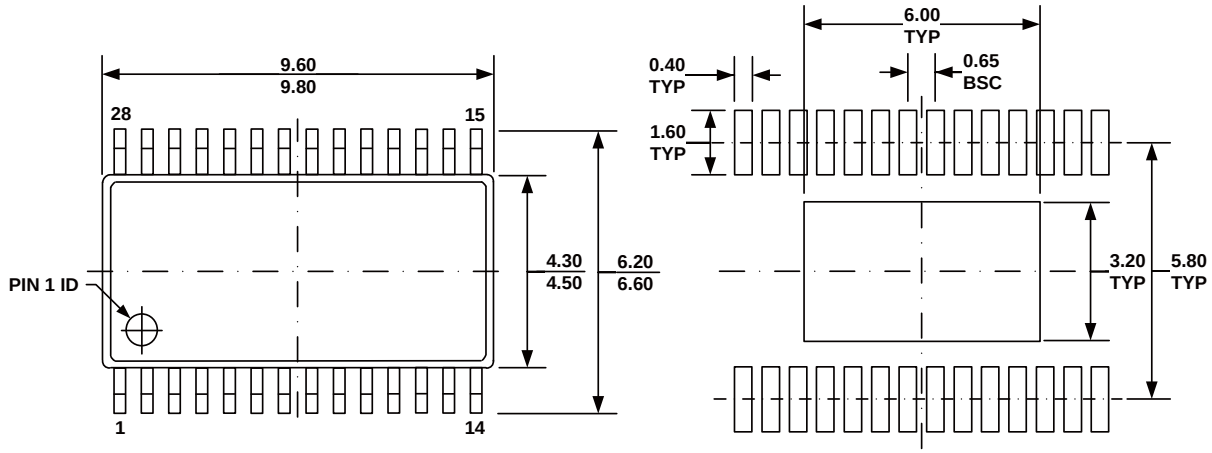
Table 2: Commutation Table (nBRAKE=1)

Logic Inputs				Driver Outputs						Motor Terminals		
HA	HB	HC	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SHA	SHB	SHC
1	0	1	1	/PWM	0	1	PWM	0	0	H	Z	L
1	0	0	1	0	/PWM	1	0	PWM	0	Z	H	L
1	1	0	1	1	/PWM	0	0	PWM	0	L	H	Z
0	1	0	1	1	0	/PWM	0	0	PWM	L	Z	H
0	1	1	1	0	1	/PWM	0	0	PWM	Z	L	H
0	0	1	1	/PWM	1	0	PWM	0	0	H	L	Z
1	0	1	0	1	0	/PWM	0	0	PWM	L	Z	H
1	0	0	0	0	1	/PWM	0	0	PWM	Z	L	H
1	1	0	0	/PWM	1	0	PWM	0	0	H	L	Z
0	1	0	0	/PWM	0	1	PWM	0	0	H	Z	L
0	1	1	0	0	/PWM	1	0	PWM	0	Z	H	L
0	0	1	0	1	/PWM	0	0	PWM	0	L	H	Z

Note: If nBRAKE=0, the braking function would be active, all low-side gates on.

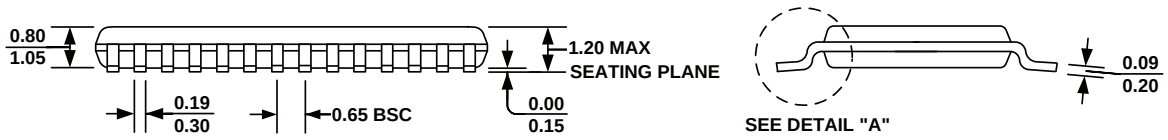
PACKAGE INFORMATION

TSSOP-28 EP



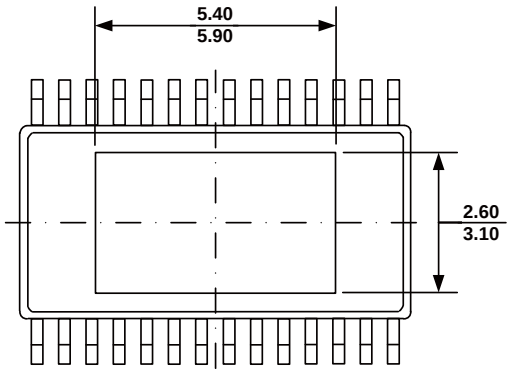
TOP VIEW

RECOMMENDED LAND PATTERN

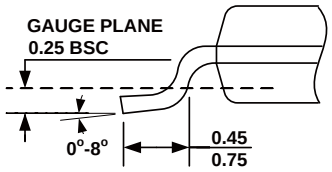


FRONT VIEW

SIDE VIEW



BOTTOM VIEW



DETAIL A

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.