56F8323

Evaluation Module User Manual

56F8300
16-bit Digital Signal Controllers

MC56F8323EVMUM
Rev. 2
07/2005

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semiconductor

Document Revision History

Version History	Description of Change
Rev 1.0	Initial Public Release
Rev 2.0	Updated look and feel

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Preface

This reference manual describes in detail the hardware on the 56F8323 Evaluation Module.

Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F8323 part.

Organization

This manual is organized into two chapters and two appendixes.

- **Chapter 1, Introduction** - provides an overview of the EVM and its features.
- **Chapter 2, Technical Summary** - describes in detail the 56F8323EVM hardware.
- **Appendix A, 56F8323EVM Schematics** - contains the schematics of the 56F8323EVM.
- **Appendix B, 56F8323EVM Bill of Material** - provides a list of the materials used on the 56F8323EVM board.

Suggested Reading

More documentation on the 56F8323 and the 56F8323EVM kit may be found at URL:

www.freescale.com

Notation Conventions

This manual uses the following notational conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	$\overline{WE}$ $\overline{OE}$	In schematic drawings, Active Low Signals may be noted by a back-slash: /WE
Hexadecimal Values	Begin with a “$” symbol	$0FF0 $80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter “b” attached to the number	b1010 b0011	
Numbers	Considered positive unless specifically noted as a negative value	5 -10	Voltage is often shown as positive: +3.3V
Blue Text	Linkable on-line	...refer to Chapter 7, License	
Bold	Reference sources, paths, emphasis	...see: **www.freescale.com**	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

A/D	Analog-to-Digital; a method of converting Analog signals to Digital values
ADC	Analog-to-Digital Converter; a peripheral on the 56F8323 part
CAN	Controller Area Network; a serial communications peripheral and method
CiA	CAN in Automation; an international CAN user's group that coordinates standards for CAN communications protocols
CTS	Clear To Send
D/A	Digital-to-Analog; a method of converting Digital values to an Analog form
56F8323	A 16-bit controller with motor control peripherals
EOnCE	Enhanced On-Chip Emulation; a debug bus and port created by Freescale to enable a designer to create a low-cost hardware interface for a professional-quality debug environment
EVM	Evaluation Module; a hardware platform which allows a customer to evaluate the silicon and develop his application
Flash	Nonvolatile Random Access Memory
FlexCAN	Flexible CAN Interface Module; a peripheral on the 56F8323 part
GPIO	General Purpose Input and Output port on Freescale's family of controllers; does not share pin functionallity with any other peripheral on the chip and can only be set as an input, output, or level-sensitive interrupt input
IC	Integrated Circuit
JTAG	Joint Test Action Group; a bus protocol/interface used for test and debug
LED	Light Emitting Diode
LQFP	Low-profile Quad Flat Package
MPIO	Multi-Purpose Input and Output port on Freescale's family of controllers; shares package pins with other peripherals on the chip and can function as a GPIO

OnCE	On-Chip Emulation, a debug bus and port created by Freescale to allow a means for low-cost hardware which provides a professional-quality debug environment
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
Quad Dec	Quadrature Decoder; a peripheral on the 56F8323 part
RAM	Random Access Memory
R/C	Resistor/Capacitor Network
SRAM	Static Random Access Memory
RTS	Request to Send
SCI	Serial Communications Interface; a peripherial on Freescale's family of controllers
SPI	Serial Peripheral Interface; a peripheral on Freescale's family of controllers
UART	Universal Asynchronous Receiver/Transmitter
WS	Wait State

References

The following sources were referenced to produce this manual:

[1] *DSP56800E Reference Manual*, DSP56800ERM; Freescale Semiconductor

[2] *56F8300 Peripheral User Manual*, MC56F8300UM; Freescale Semiconductor

[3] *56F8323 Technical Data*, MC56F8323; Freescale Semiconductor

[4] *CiA Draft Recommendation DR-303-1, Cabling and Connector Pin Assignment*, Version 1.0, CAN in Automation

[5] *CAN Specification 2.0B*, BOSCH or CAN in Automation

Chapter 1
Introduction

The 56F8323EVM is used to demonstrate the abilities of the 56F8323 and to provide a hardware tool allowing the development of applications that use the 56F8323.

The 56F8323EVM is an evaluation module board that includes an 56F8323 part, peripheral expansion connectors, a CAN interface, an RS-232 interface, a JTAG-to-PC Printer port interface and a pair of daughter card connectors. The peripheral expansion connectors and daughter card expansion connectors are for signal monitoring and allow expansion for user features.

The 56F8323EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800E architecture. The tools and examples provided with the 56F8323EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip SRAM or Flash, run it, and debug it using a debugger via the JTAG/Enhanced OnCE (EOnCE) port. The breakpoint features of the EOnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full speed until the break conditions are satisfied. The ability to examine and modify all user-accessible registers, memory and peripherals through the EOnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the controller's peripherals. The EOnCE port's unobtrusive design means that all memory on the Processor is available to the user.

1.1 56F8323EVM Architecture

The 56F8323EVM facilitates the evaluation of various features present in the 56F8323 part. The 56F8323EVM can be used to develop real-time software and hardware products based on the 56F8323. The 56F8323EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the user's application-specific device(s). The 56F8323EVM is flexible enough to allow a user to fully exploit the 56F8323's features to optimize the performance of his product, as shown in **Figure 1-1**.

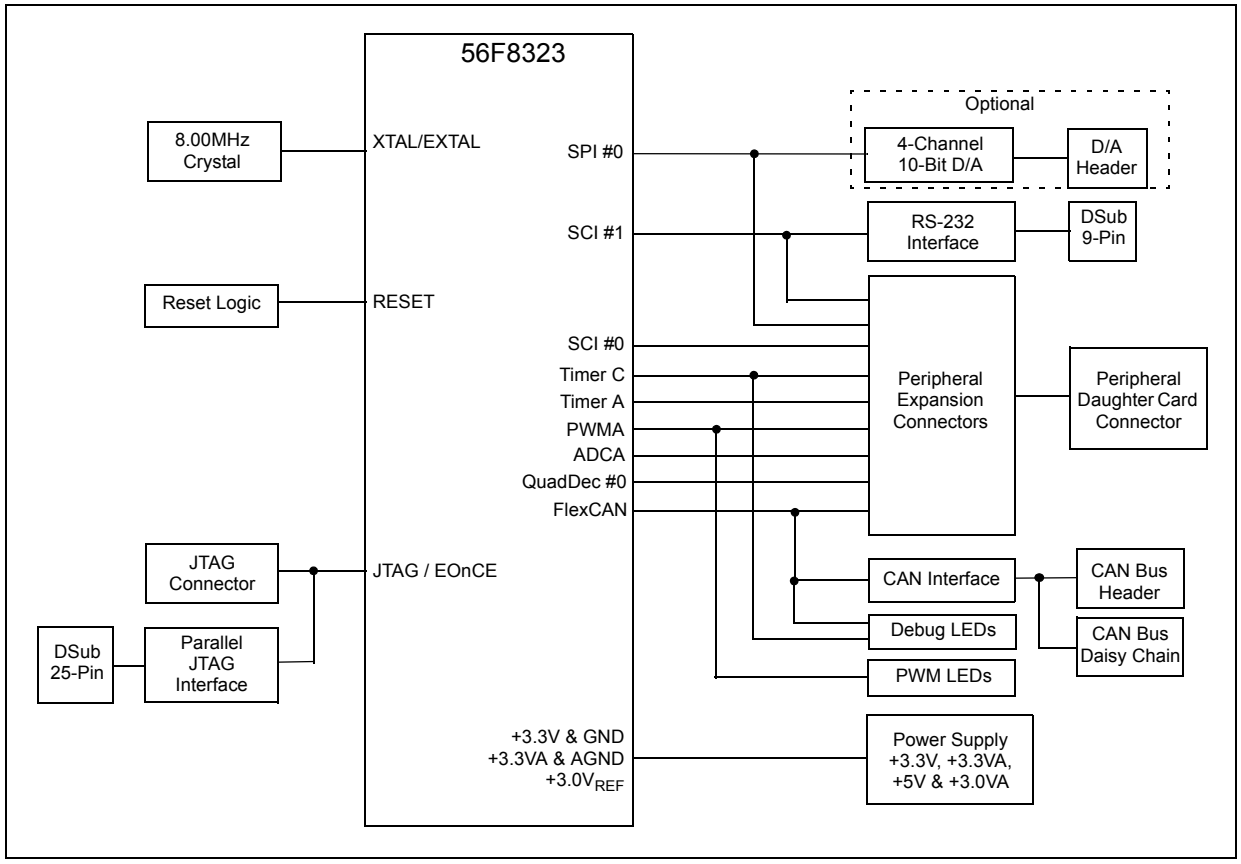

Figure 1-1. Block Diagram of the 56F8323EVM

1.2 56F8323EVM Configuration Jumpers

Fifteen jumper groups, (JG1-JG15), shown in **Figure 1-2**, are used to configure various features on the 56F8323EVM board. **Table 1-1** describes the default jumper group settings.

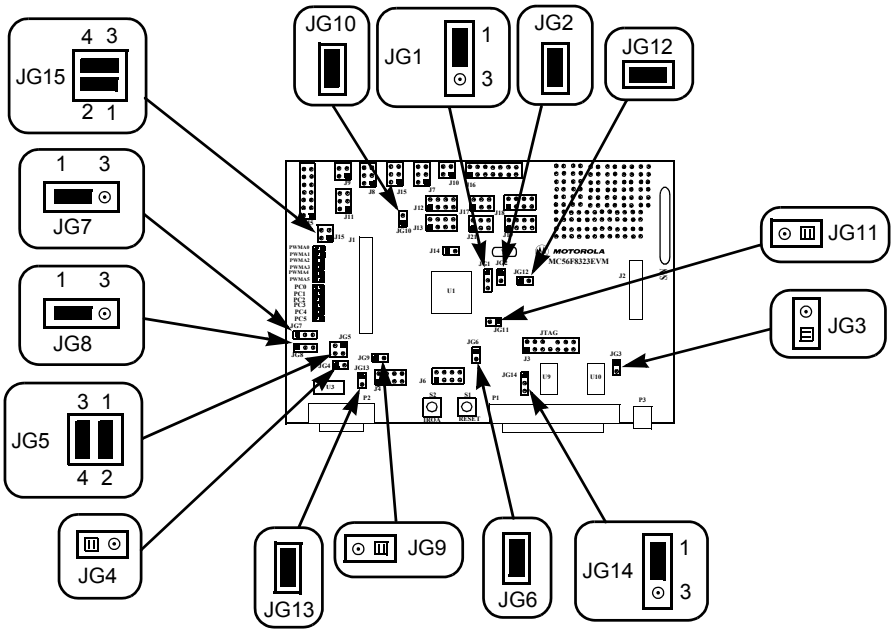

Figure 1-2. 56F8323EVM Jumper Reference

Table 1-1. 56F8323EVM Default Jumper Options

Jumper Group	Comment	Jumpers Connections
JG1	Connect on-board 8.0MHz crystal input to EXTAL signal	1–2
JG2	Connect on-board 8.0MHz crystal input to XTAL signal	1–2
JG3	Enable on-board Parallel JTAG Host/Target Interface	NC
JG4	Enable RS-232 output	NC
JG5	Pass RXD1 & TXD1 signals to RS-232 level converter	1–2 & 3–4
JG6	Pass Temperature Diode signal to ANA7 input	1–2
JG7	Set user Jumper #0 to a 1 value	1–2
JG8	Set user Jumper #1 to a 1 value	1–2
JG9	SPI #0 Daisy Chain (Optional--not populated on board by default)	NC
JG10	CAN bus termination selected	1–2
JG11	Connect Analog Ground to Digital Ground	NC
JG12	Enable on-chip regulator	1–2
JG13	Pass RTS to CTS	1–2
JG14	Select +3.3V operation of on-board Parallel JTAG Host/Target Interface	1–2
JG15	Pass CAN_TX & CAN_RX signals to CAN tranceiver	1–2 & 3–4

1.3 56F8323EVM Connections

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and the external +12.0V DC/AC power supply to the 56F8323EVM board.

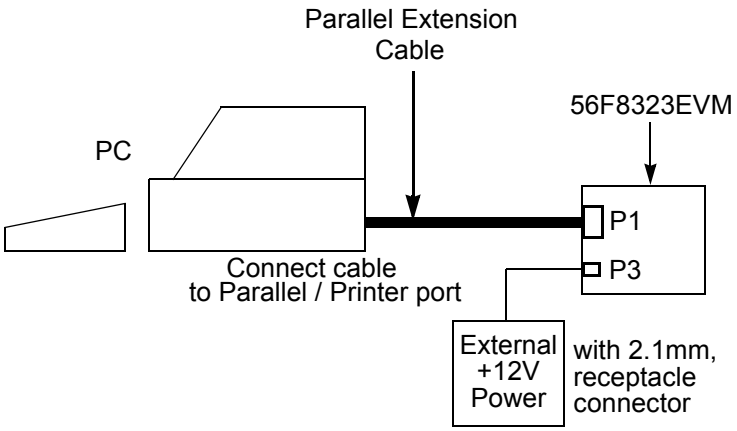

Figure 1-3. Connecting the 56F8323EVM Cables

Perform the following steps to connect the 56F8323EVM cables:

1. Connect the parallel extension cable to the Parallel port of the host computer.
2. Connect the other end of the parallel extension cable to P1, shown in **Figure 1-3**, on the 56F8323EVM board. This connection allows the host computer to control the board.
3. Make sure that the external +12V DC, 1.2A power supply is not plugged into a +120V AC power source.
4. Connect the 2.1mm output power plug from the external power supply into P3, shown in **Figure 1-3**, on the 56F8323EVM board.
5. Apply power to the external power supply. The green Power-On LED, LED13, will illuminate when power is correctly applied.

Chapter 2
Technical Summary

The 56F8323EVM is designed as a versatile Flash-based microcontroller development card for developing real-time software and hardware products to support a new generation of applications in servo and motor control; digital and wireless messaging; digital answering machines; feature phones; modems; and digital cameras. The power of the 16-bit 56F8323, combined with the on-board RS-232 interface, CAN interface, Daughter Card Expansion interface and parallel JTAG interface, makes the 56F8323EVM ideal for developing and implementing many motor controlling algorithms, as well as for learning the architecture and instruction set of the 56F8323 processor.

The main features of the 56F8323EVM, with board and schematic reference designators, include:

- MC56F8323, a 16-bit +3.3V/+2.5V processor in a 64-pin LQFP package operating at 60MHz [U1]
- 8.00MHz crystal oscillator for processor frequency generation [Y1]
- Optional external oscillator frequency input connectors [JG1 and JG2]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J3]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P1], including a disable jumper [JG3]
- On-board Parallel JTAG Host Taget Interface voltage level selector [JG14]
- RS-232 interface for easy connection to a host processor [U3 and P2], with a disable jumper [JG4]
- RS-232 RTS and CTS signal connector [JG13]
- CAN interface for high speed, 1.0Mbps, FlexCAN communications [U8 and J12]
- CAN bypass and bus termination [J13 and JG10]
- CAN signal to CAN transceiver isolation connector [JG15]
- Peripheral Daughter Card Expansion Connector, which allows the user to attach his own SCI, SPI, PWM, Quad Decoder or GPIO-compatible peripherals to the Processor [J1]

- Memory Daughter Card Expansion Connector, which allows the user to attach additonal power and grounds[J2]
- Connector which allows the user to attach his own SCI #0 / MPIO-compatible peripheral [J21]
- Connector which allows the user to attach his own SCI #1 / MPIO-compatible peripheral [J17]
- Connector which allows the user to attach his own SPI #0 / MPIO-compatible peripheral [J8]
- Connector which allows the user to attach his own SPI #1 / MPIO-compatible peripheral [J15]
- Connector which allows the user to attach his own PWMA-compatible peripheral [J5]
- Connector which allows the user to attach his own CAN physical layer peripheral [J10]
- Connector which allows the user to attach his own Timer A / Encoder #0-compatible peripheral [J7]
- Connector which allows the user to attach his own Timer C-compatible peripheral [J9]
- Connector which allows the user to attach his own A/D port A-compatible peripheral [J6]
- Connector which allows the user to attach his own peripheral to GPIO Port A [J16]
- Connector which allows the user to attach his own peripheral to GPIO Port B [J18]
- Connector which allows the user to attach his own peripheral to GPIO Port C [J19]
- On-board power regulation from an external +12V DC-supplied power input [P3]
- Light Emitting Diode (LED) power indicator [LED13]
- Six on-board LEDs allow real-time debugging of user programs [LED1-6]
- Six on-board Port A PWM monitoring LEDs [LED7-12]
- Internal (OCR_DIS) Core Regulator selector [JG12]
- Temperature Sense Diode-to-ANA7 selector [JG6]
- Manual RESET push-button [S1]
- Manual interrupt push-button for $\overline{\text{IRQA}}$ [S2]
- General purpose jumper on GPIO PB3 [JG7]
- General purpose jumper on GPIO PB0 [JG8]
- Optional 4-Channel 10-bit Serial D/A, SPI for real-time user data display [U5]

2.1 56F8323

The 56F8323EVM uses a Freescale MC56F8323 part, designated as U1 on the board and in the schematics. This part will operate at a maximum external bus speed of 60MHz. A full description of the 56F8323, including functionality and user information, is provided in these documents:

- 56F8323 *Technical Data Sheet*, (MC56F8323)**:** Electrical and timing specifications, pin descriptions, device specific peripheral information and package descriptions (this document)
- *56F8300 Peripheral User Manual*, (MC56F8300UM): Detailed description of peripherals of the 56F8300 family of devices
- *DSP56800E Reference Manual*, (DSP56800ERM): Detailed description of the 56800E family architecture, 16-bit core processor, and the instruction set

Refer to these documents for detailed information about chip functionality and operation. They can be found on this URL:

www.freescale.com

2.2 RS-232 Serial Communications

The 56F8323EVM provides an RS-232 interface by the use of an RS-232 level converter, Maxim MAX3245EEAI, designated as U3. Refer to the RS-232 schematic diagram in **Figure 2-1**. The RS-232 level converter transitions the SCI UART's +3.3V signal levels to RS-232-compatible signal levels and connects to the host's serial port via connector P2. Flow control is not provided, but could be implemented using uncommitted GPIO signals and connected to the RTS and CTS signals on JG13; see **Table 2-1**. The SCI1 port signals can be isolated from the RS-232 level converter by removing the jumpers in JG5; reference **Table 2-2**. The pin-out of connector P2 is detailed in **Table 2-3**. The RS-232 level converter/transceiver can be disabled by placing a jumper at JG4.

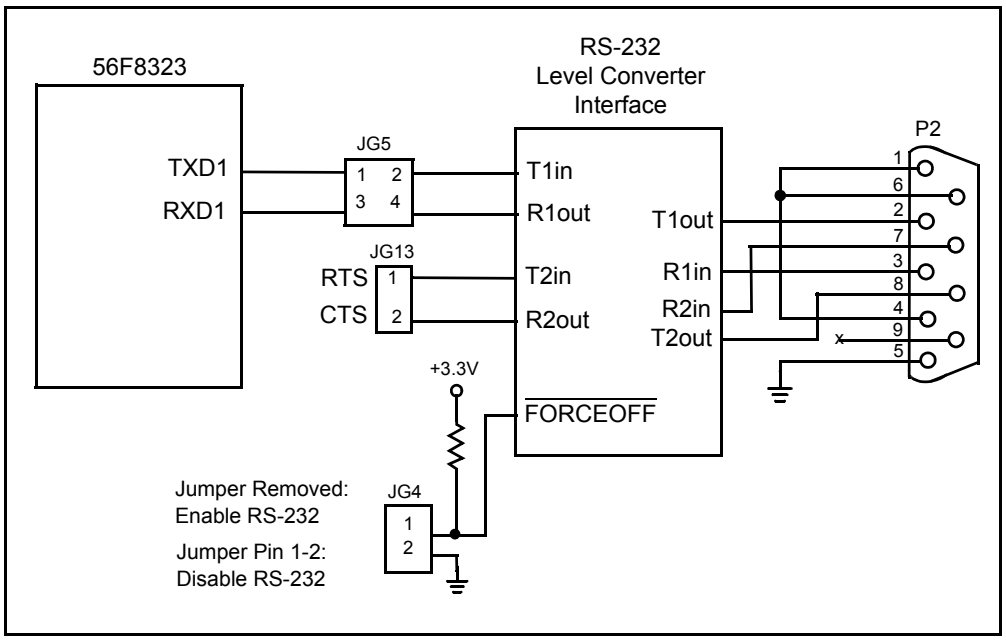

Figure 2-1. Schematic Diagram of the RS-232 Interface

Table 2-1. Flow Control Header Options

JG13	
Pin #	**Signal**
1	RTS to Transceiver
2	CTS from Transceiver

Table 2-2. SCI1 Jumper Options

JG5			
Pin #	**Signal**	**Pin #**	**Signal**
1	TXD1	2	TXD to RS-232 Transceiver
3	RXD1	4	RXD from RS-232 Transceiver

Table 2-3. RS-232 Serial Connector Description

P2			
Pin #	**Signal**	**Pin #**	**Signal**
1	Jumper to 6 & 4	6	Jumper to 1 & 4
2	TXD	7	CTS
3	RXD	8	RTS
4	Jumper to 1 & 6	9	NC
5	GND		

The 56F8323EVM uses on-chip 8.00MHz relaxation oscillator or the on-board 8.00MHz crystal, Y1, connected to its External Crystal Inputs, EXTAL and XTAL. To achieve its maximum internal operating frequency, the 56F8323 uses its internal PLL to multiply this input clock frequency. Additionally an external oscillator source can be connected to the device by using the oscillator bypass connectors, JG1 and JG2; see **Figure 2-2**. If the input frequency is above 8MHz, then the EXTAL input should be jumpered to ground by adding a jumper between JG1 pins 2 and 3. The input frequency would then be injected on JG2's pin 2. If the input frequency is below 4MHz, then the input frequency can be injected on JG1's pin 2.

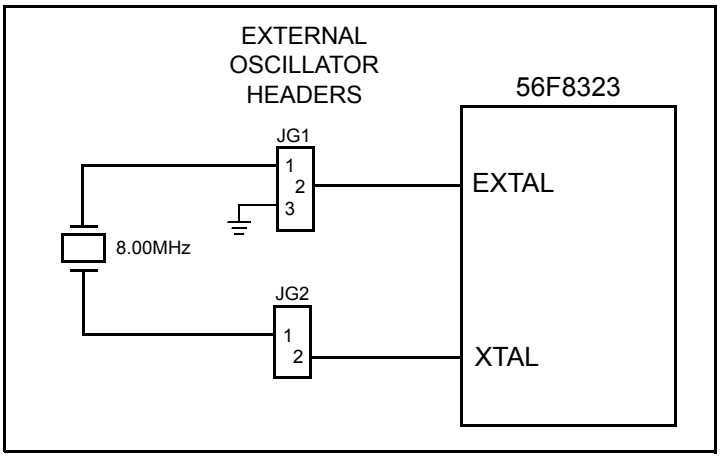

Figure 2-2. Schematic Diagram of the Clock Interface

Six on-board Light-Emitting Diodes, (LEDs), are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging; refer to **Figure 2-3**. **Table 2-4** describes the control of each LED.

Table 2-4. LED Control

	Controlled by	
User LED	**Color**	**Signal**
LED1	RED	GPIO Port C Bit 0
LED2	YELLOW	GPIO Port C Bit 1
LED3	GREEN	GPIO Port C Bit 2
LED4	RED	GPIO Port C Bit 3
LED5	YELLOW	GPIO Port C Bit 4
LED6	GREEN	GPIO Port C Bit 5

Setting PC0, PC1, PC2, PC3, PC4 or PC5 to a Logic One value will turn on the associated LED.

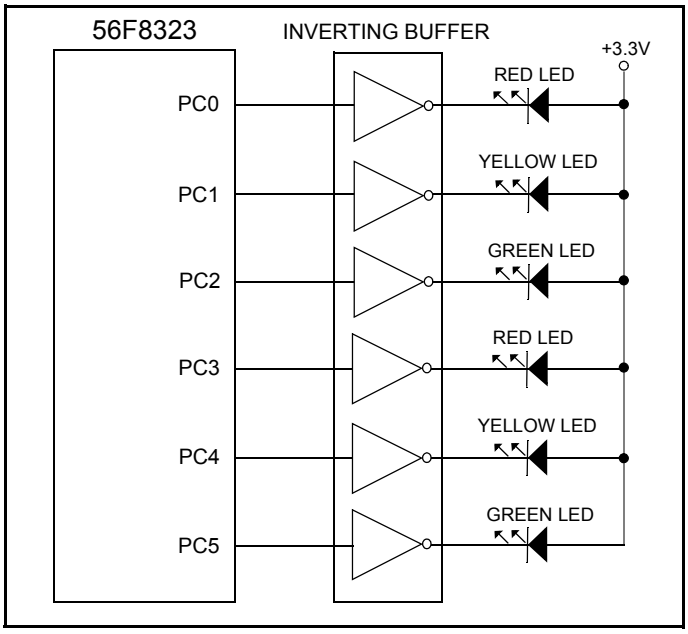

Figure 2-3. Schematic Diagram of the Debug LED Interface

2.3 Debug Support

The 56F8323EVM provides an on-board Parallel JTAG Host Target Interface and a JTAG interface connector for external Target Interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the Host Parallel Interface Connector.

2.3.1 JTAG Connector

The JTAG connector on the 56F8323EVM allows the connection of an external Host Target Interface for downloading programs and working with the 56F8323's registers. This connector is used to communicate with an external Host Target Interface which passes information and data back and forth with a host processor running a debugger program. **Table 2-5** shows the pin-out for this connector.

Table 2-5. JTAG Connector Description

J3			
Pin #	**Signal**	**Pin #**	**Signal**
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NC	8	KEY
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V	12	NC
13	$\overline{\text{DE}}$	14	$\overline{\text{TRST}}$

When this connector is used with an external Host Target Interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG3. Refer to **Table 2-6** for this jumper's selection options.

Table 2-6. Parallel JTAG Interface Disable Jumper Selection

JG3	Comment
No jumpers	Enable On-board Parallel JTAG Interface
1–2	Disable on-board Parallel JTAG Interface

2.3.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P1, allows the 56F8323 to communicate with a Parallel Printer Port on a Windows PC; reference **Figure 2-4**. Using this connector, the user can download programs and work with the 56F8323's registers. **Table 2-7** shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG3 should be removed, as shown in **Table 2-6**. A jumper at JG14 selects the Parallel Printer Port's interface voltage between +3.3V and +5.0V; see **Table 2-8**.

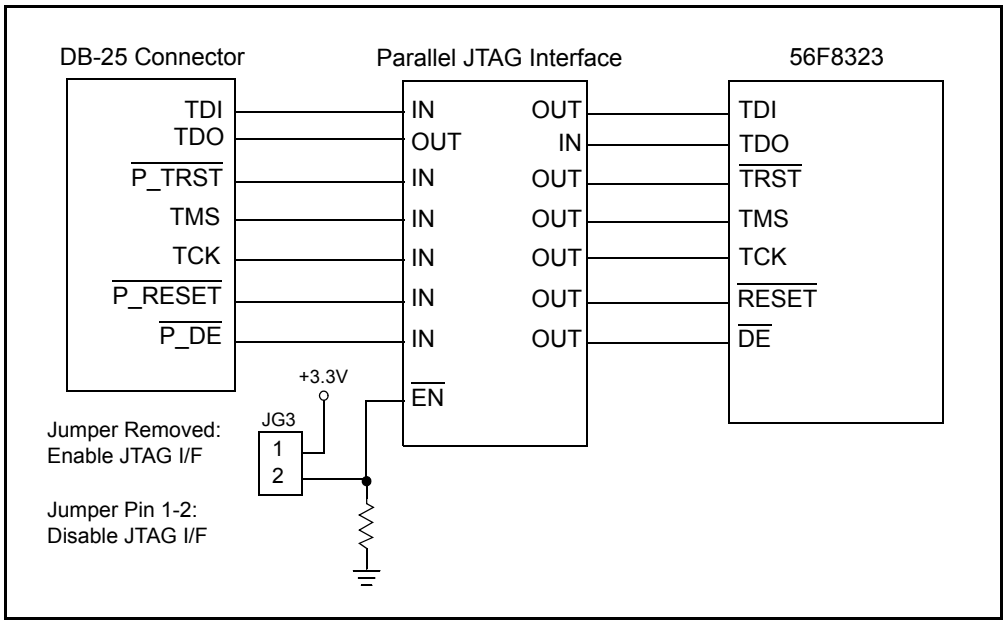

Figure 2-4. Block Diagram of the Parallel JTAG Interface

Table 2-7. Parallel JTAG Interface Connector Description

P1			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	14	NC
2	PORT_RESET	15	PORT_IDENT
3	PORT_TMS	16	N/C
4	PORT_TCK	17	N/C
5	PORT_TDI	18	GND
6	$\overline{\text{PORT\_TRST}}$	19	GND
7	$\overline{\text{PORT\_DE}}$	20	GND
8	PORT_IDENT	21	GND
9	PORT_VCC	22	GND
10	NC	23	GND
11	PORT_TDO	24	GND
12	NC	25	GND
13	PORT_CONNECT		

Table 2-8. Parallel JTAG Interface Voltage Selection Jumper

JG14	Comment
1–2	+3.3V Parallel Printer Port Interface
2–3	+5.0V Parallel Printer Port Interface

2.4 External Interrupts

One on-board push-button switch is provided for external interrupt generation, as shown in **Figure 2-5**. S2 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$. This switch allows the user to generate interrupts for user-specific programs.

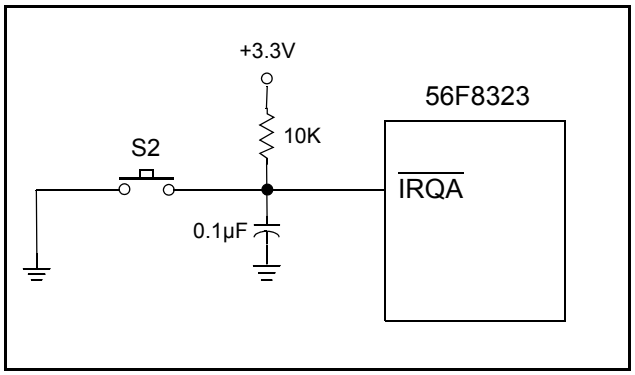

Figure 2-5. Schematic Diagram of the User Interrupt Interface

2.5 Reset

Logic is provided on the 56F8323 to generate an internal Power-On RESET. Additional reset logic is provided to support the RESET signals from the JTAG connector, the Parallel JTAG Interface and the user RESET push-button, S1; refer to **Figure 2-6**.

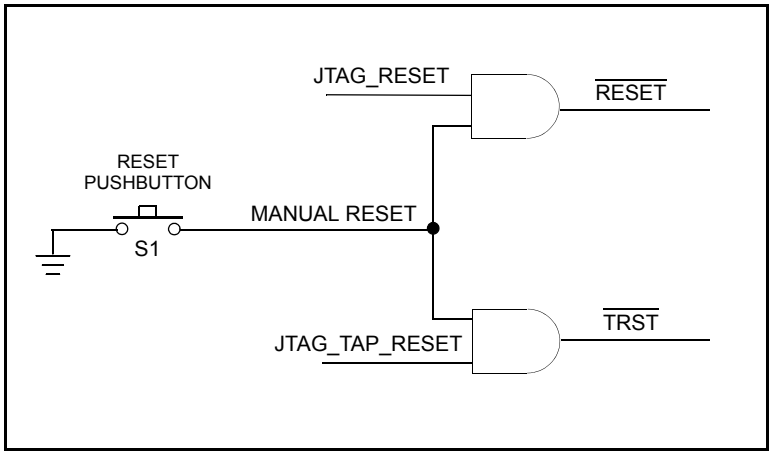

Figure 2-6. Schematic Diagram of the RESET Interface

2.6 Power Supply

The main power input to the 56F8323EVM, +12V DC at 1.2A, is through a 2.1mm coax power jack. This input power is rectified to provide a DC supply input. This allows a user the option to use a +12V AC power supply. A 1.2Amp power supply is provided with the 56F8323EVM; however, less than 500mA is required by the EVM. The remaining current is available for custom control applications when connected to the Daughter Card connectors. The 56F8323EVM provides +5.0V DC regulation for the CAN interface and additional regulators. The 56F8323EVM provides +3.3V DC voltage regulation for the processor, memory, D/A, ADC, parallel JTAG interface and supporting logic; refer to **Figure 2-7**. Additional voltage regulation logic provides a low noise +3.0V DC voltage reference to the controller's A/D V_{REFH}. Optionally, the processor's A/D V_{REFH} voltage can be provided by the +3.3VA supply on the board by removing U15 and adding a 10 ohm resistor at R83. A jumper, JG11, and resistor, R68, are provided to allow the analog and digital grounds to be isolated on the 56F8323EVM board. This allows the analog ground reference point to be provided on a custom board attached to the 56F8323EVM's Daughter Card connectors. By removing R68, the AGND reference is disconnected from the 56F8323EVM's digital ground. By placing a jumper in JG11 or by reinstalling R68, the AGND is reconnected to the 56F8323EVM's digital ground. Power applied to the 56F8323EVM is indicated with a Power-On LED, referenced as LED13. Optionally, the user can provide the +2.5 DC voltage needed by the controller's core on connector J14 and disable the on-chip CORE voltage regulator by removing the jumper on JG12. Additonally, four 0 ohm resistors or shorting wires must be added at R70, R71, R72 and R73, to allow the external +2.5V DC to pass to the 56F8323.

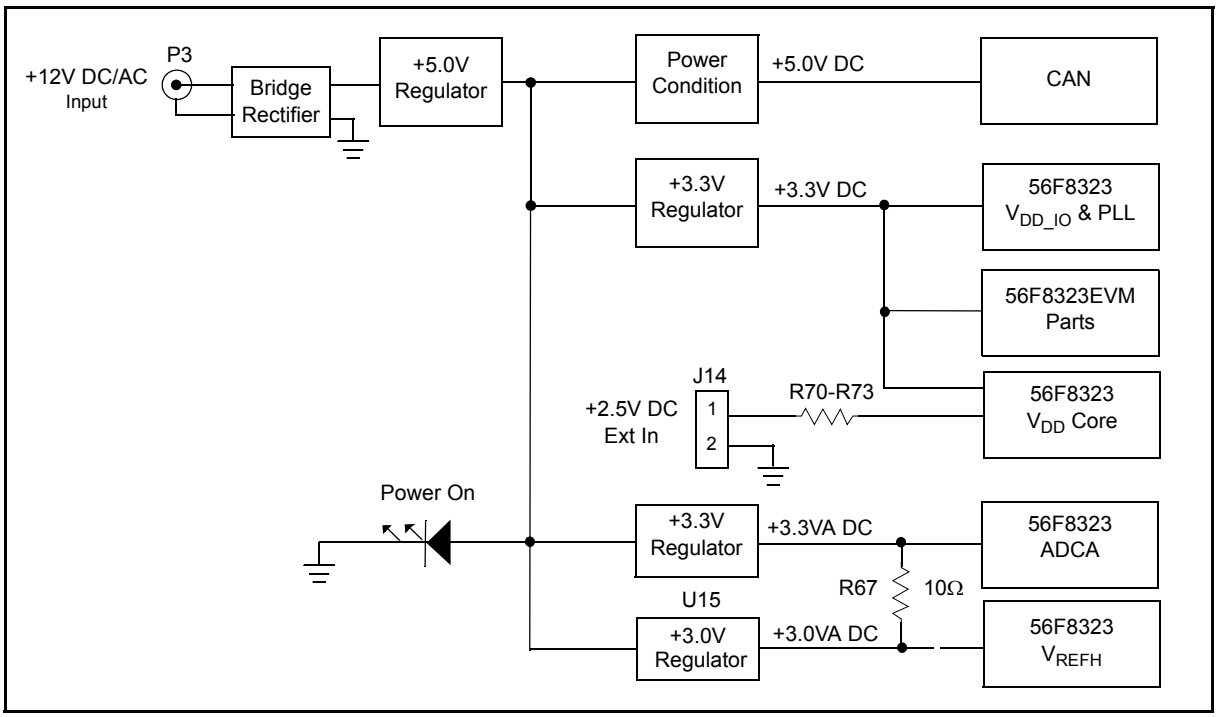

Figure 2-7. Schematic Diagram of the Power Supply

2.7 Daughter Card Connectors

The EVM board contains two daughter card expansion connectors. One connector, J1, contains the processor's peripheral port signals. The second connector, J2, contains addional power and ground signals.

2.7.1 Peripheral Daughter Card Expansion Connector

The processor's peripheral port signals are connected to the Peripheral Daughter Card Expansion connector, J1. The Peripheral Daughter Card connector is used to connect a user-specific daughter card to the processor's peripheral port signals. The Peripheral Port Daughter Card connector is a 100-pin high-density connector with signals for the IRQs, RESET, SPI, SCI, PWM, ADC and Quad Timer ports. **Table 2-9** shows the Peripheral Daughter Card connector's signal-to-pin assignments.

Table 2-9. Peripheral Daughter Card Connector Description

J1			
Pin #	**Signal**	**Pin #**	**Signal**
1	+12V	2	+12V
3	GND	4	GND
5	+5.0V	6	+5.0V
7	GND	8	GND
9	+3.3V	10	+3.3V
11	GND	12	GND
13	NC	14	NC
15	NC	16	NC
17	GND	18	GND
19	PHASEA0 / PB7 / TA0	20	PHASEB0 / PB6 / TA1
21	INDEX0 / PB5 / TA2	22	HOME0 / PB4 / TA3
23	TC0	24	$\overline{SS0}$
25	TC0	26	$\overline{SS0}$
27	TC1	28	MISO0

Table 2-9. Peripheral Daughter Card Connector Description (Continued)

J1			
Pin #	**Signal**	**Pin #**	**Signal**
29	$\overline{\text{IRQA}}$	30	NC
31	TC1	32	TC3
33	PWMA0	34	PWMA1
35	PWMA2	36	PWMA3
37	PWMA4	38	PWMA5
39	GND	40	GND
41	ISA0	42	ISA1
43	ISA2	44	GND
45	FAULTA1	46	FAULTA0
47	NC	48	FAULTA2
49	GND	50	GND
51	NC	52	MISO0
53	NC	54	NC
55	NC	56	NC
57	GND	58	GND
59	NC	60	NC
61	NC	62	$\overline{\text{SS0}}$
63	NC	64	NC
65	NC	66	NC
67	MOSI0	68	$\overline{\text{SS0}}$
69	TC0	70	TC1
71	SCLK0	72	TC0
73	CAN_TX	74	CAN_RX
75	MOSI0	76	MISO0
77	SCLK0	78	$\overline{\text{SS0}}$

Table 2-9. Peripheral Daughter Card Connector Description (Continued)

J1			
Pin #	**Signal**	**Pin #**	**Signal**
79	GND	80	GND
81	$+V_{REFH}$	82	$+V_{REFH}$
83	GNDA	84	GNDA
85	NC	86	NC
87	NC	88	NC
89	NC	90	NC
91	NC	92	NC
93	AN0	94	AN1
95	AN2	96	AN3
97	AN4	98	AN5
99	AN6	100	AN7

2.7.2 Memory Daughter Card Expansion Connector

Additional power and ground signals are connected to the Memory Daughter Card Expansion connector, J2. **Table 2-10** shows the port signal-to-pin assignments.

Table 2-10. Memory Daughter Card Connector Description

J2			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	GND	10	GND
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	GND	20	GND
21	GND	22	GND
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC
31	GND	32	GND
33	GND	34	GND
35	NC	36	NC
37	NC	38	NC
39	NC	40	NC
41	NC	42	NC

Table 2-10. Memory Daughter Card Connector Description (Continued)

J2			
Pin #	**Signal**	**Pin #**	**Signal**
43	GND	44	GND
45	NC	46	NC
47	NC	48	NC
49	NC	50	NC
51	NC	52	GND
53	GND	54	GND
55	+3.3V	56	+3.3V
57	GND	58	GND
59	+5.0V	60	+5.0V

2.8 Serial 10-bit 4-channel D/A Converter (Optional)

The 56F8323EVM board contains the provions for a user to provide a serial 10-bit, 4-channel D/A converter connected to the 56F8323's SPI #0 port. The output pins are uncommitted and are connected to a 4x2 header, J4, to allow easy user connections. Refer to **Figure 2-8** for the D/A connections and **Table 2-11** for the header's pin-out. The D/A's output full-scale range value can be set to a value from +0.0V to +2.4V by a trimpot, R48. If this trimpot is preset to +2.05V, it would provide approximately +2mV per step. If another device must be used with SPI #0's MISO signal and with the D/A converter on the board, the daisy chain jumper, JG9, can be used to extend or isolate the serial chain.

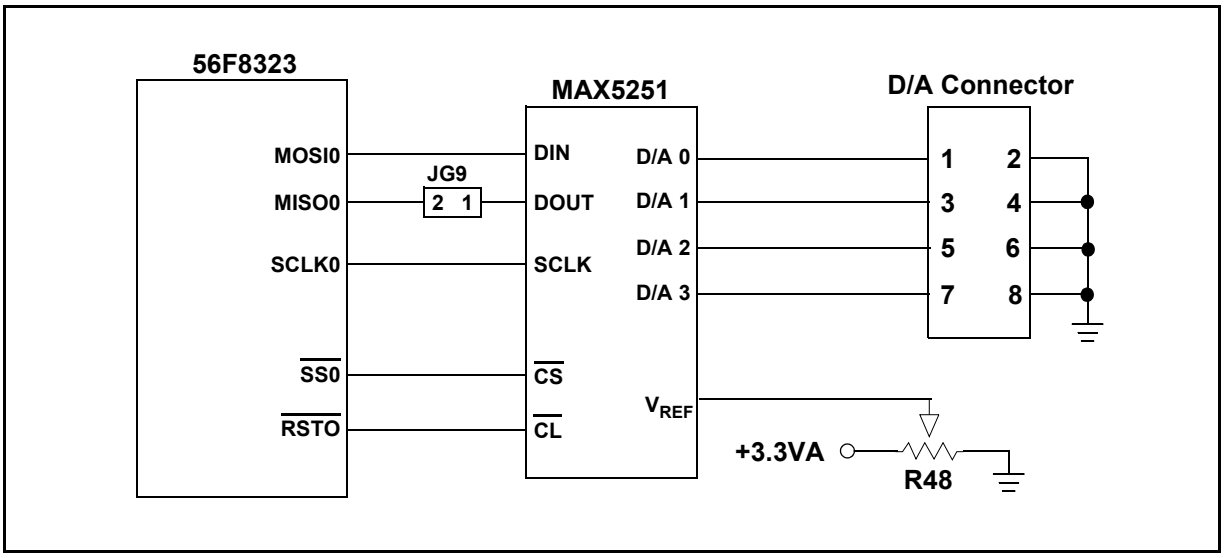

Figure 2-8. Serial 10-bit, 4-Channel D/A Converter

Table 2-11. D/A Header Description

J4			
Pin #	**Signal**	**Pin #**	**Signal**
1	D/A Channel 0	2	AGND
3	D/A Channel 1	4	AGND
5	D/A Channel 2	6	AGND
7	D/A Channel 3	8	AGND

2.9 Motor Control PWM Signals and LEDs

The 56F8323 has one PWM unit. This unit contains six PWM output signals, three Fault input signals and three Phase Current sense inputs. The PWM signals are connected to a set of six PWM LEDs via inverting buffers. The buffers are used to isolate and drive the processor's PWM outputs to the PWM LEDs. The PWM LEDs indicate the status of PWM signals; refer to **Figure 2-9**. Additionally, the PWM signals are routed out to a header, J5, and to the peripheral daughter card connector, J1, for easy use by the end user.

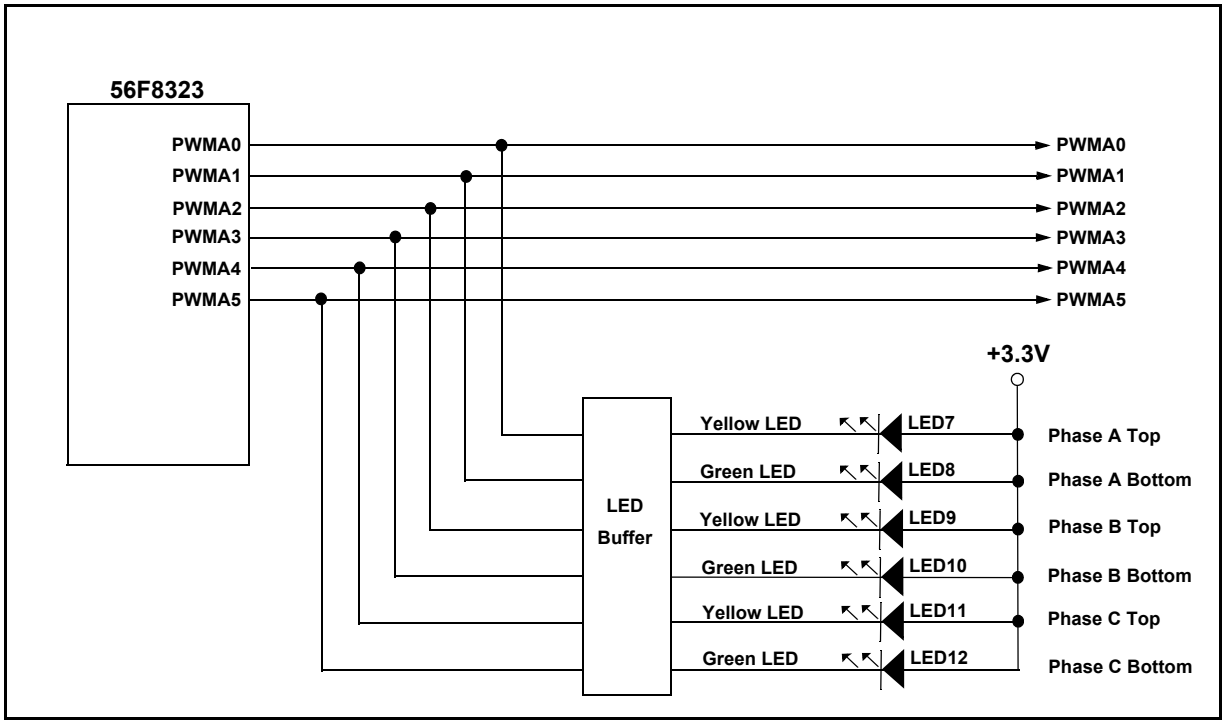

Figure 2-9. PWM Interface and LEDs

2.10 CAN Interface

The 56F8323EVM board contains a CAN physical-layer interface chip that is attached to the FlexCAN port's CAN_RX and CAN_TX pins on the 56F8323. The EVM board uses a Philips high-speed, 1.0Mbps, physical layer interface chip, PCA82C250. Due to the +5.0V operating voltage of the CAN interface chip, a pull-up to +5.0V is required to level shift the Transmit Data output line from the 56F8323. The CAN_TX and CAN_RX signals from the processor can be isolated by the connector at JG15; see **Table 2-12**. The CANH and CANL signals pass through inductors before attaching to the CAN bus connectors. A primary, J12, and daisy chain, J13, CAN connectors are provided to allow easy daisy chaining of CAN devices. CAN bus termination of 120 ohms can be provided by adding a jumper to JG10. Refer to **Table 2-13** for the CAN connector signals and to **Figure 2-10** for a connection diagram.

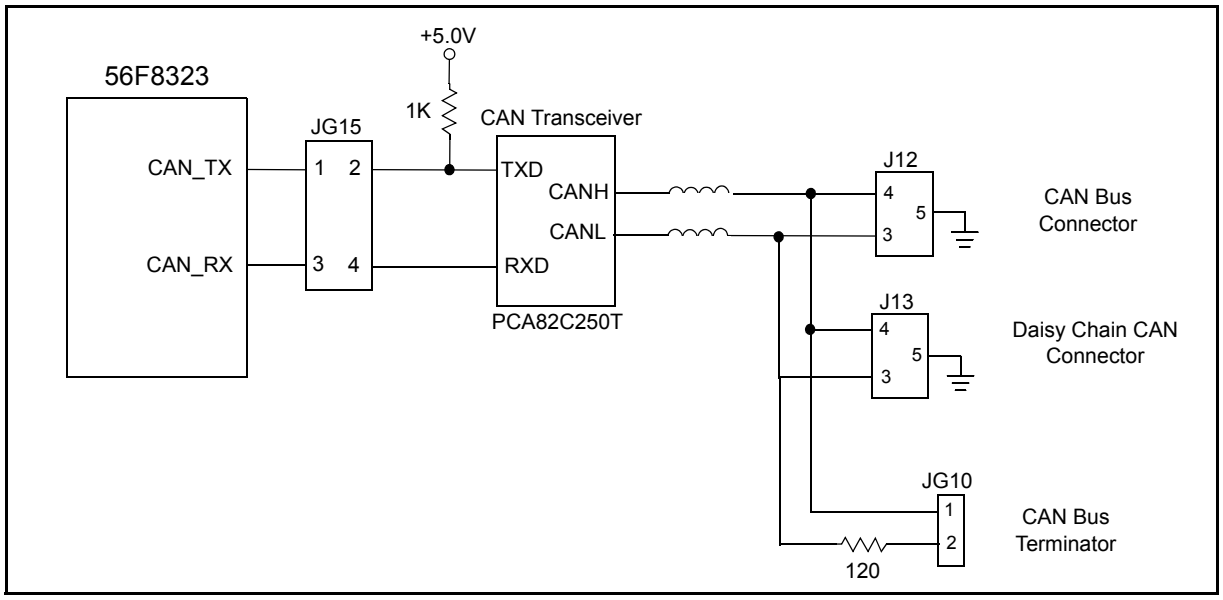

Figure 2-10. CAN Interface

Table 2-12. CAN Signal Isolation Jumper Options

JG15			
Pin #	**Signal**	**Pin #**	**Signal**
1	CAN_TX	2	CAN_TX to CAN Transceiver
3	CAN_RX	4	CAN_RX from CAN Transceiver

Table 2-13. CAN Header Description

J12 and J13			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	2	NC
3	CANL	4	CANH
5	GND	6	NC
7	NC	8	NC
9	NC	10	NC

2.11 Software Feature Jumpers

The 56F8323EVM board contains two software feature jumpers that allow the user to select "user-defined" software features. Two GPIO port pins, PB3 and PB0, are pulled high or low with 10K ohm resistors on JG7 and JG8, respectively. Attaching a jumper between pins 1 and 2 will place a high, or 1, on the port pin. Attaching a jumper between pins 2 and 3 will place a low, or 0, on the port pin; see **Figure 2-11**.

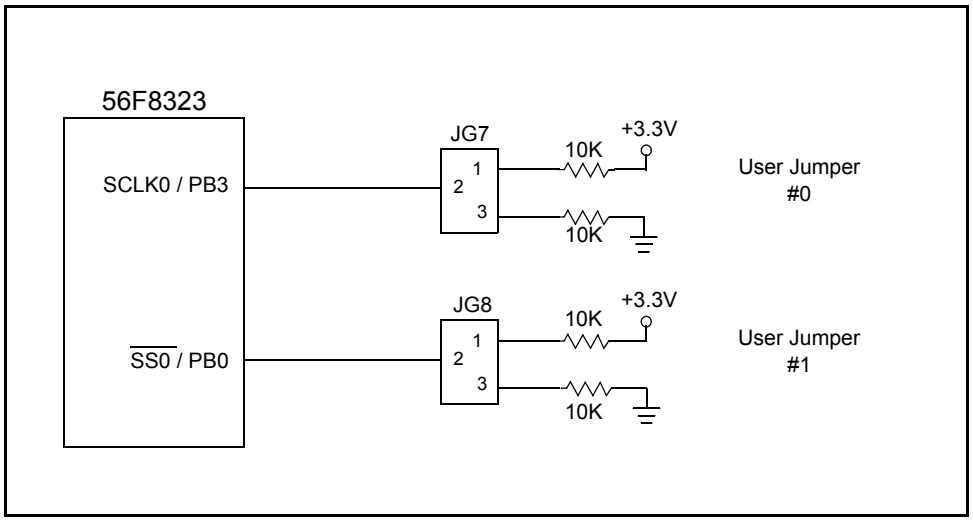

Figure 2-11. Software Feature Jumpers

2.12 Peripheral Expansion Connectors

The EVM board contains a group of Peripheral Expansion Connectors used to gain access to the resources of the 56F8323. The following signal groups have expansion connectors:

- PWM Port A
- Serial Peripheral Interface Port #0
- Serial Peripheral Interface Port #1
- Serial Communications Port 0
- Serial Communications Port 1
- Encoder #0 / Timer Channel A
- Timer Channel C
- FlexCAN Port
- A/D Input Port A
- GPIO Port A
- GPIO Port B
- GPIO Port C
- IRQA / RESET / CLOCK

2.12.1 PWM Port A Expansion Connector

The PWM port A is attached to this connector. Refer to **Table 2-14** for connection information.

Table 2-14. PWM Port A Connector Description

J5			
Pin #	**Signal**	**Pin #**	**Signal**
1	PWMA0 / PA0	2	PWMA1 / PA1
3	PWMA2 / PA2 / $\overline{SS1}$	4	PWMA3 / PA3 / MISO1
5	PWMA4 / PA4 / MOSI1	6	PWMA5 / PA5 / SCLK1
7	FAULTA0 / PA6	8	FAULTA1 / PA7
9	FAULTA2 / PA8	10	NC
11	ISA0 / PA9	12	ISA1 / PA10
13	ISA2/PA11	14	GND

2.12.2 Serial Peripheral Interface #0 Expansion Connector

The Serial Peripheral Interface #0 is an MPIO port attached to this connector. This port can be configured as a Serial Peripheral Interface or as a General Purpose I/O port. Refer to **Table 2-15** for connection information.

Table 2-15. SPI #0 Connector Description

J8			
Pin #	**Signal**	**Pin #**	**Signal**
1	MOSI0 / PB2	2	MISO0 / PB1 / RXD1
3	SCLK0 / PB3	4	$\overline{SS0}$ / PB0 / TXD1
5	GND	6	+3.3V

2.12.3 Serial Peripheral Interface #1 Expansion Connector

The Serial Peripheral Interface #1 is an MPIO port attached to this connector. This port can be configured as a Serial Peripheral Interface or as a General Purpose I/O port. Refer to **Table 2-16** for the connection information.

Table 2-16. SPI #1 Connector Description

J15			
Pin #	**Signal**	**Pin #**	**Signal**
1	MOSI1 / PWMA4	2	MISO1 / PWMA3
3	SCLK1 / PWMA5	4	$\overline{SS1}$ / PWMA2
5	GND	6	+3.3V

2.12.4 Serial Communications Port #0 Expansion Connector

The Serial Communications Port #0 is an MPIO port attached to the SCI #0 expansion connector. This port can be configured as a Serial Communications Interface or as Timer Port C channels. Refer to **Table 2-17** for connection information.

Table 2-17. SCI #0 Connector Description

J21			
Pin #	**Signal**	**Pin #**	**Signal**
1	TXD0 / TC0	2	RXD0 / TC1
3	GND	4	+3.3V
5	GND	6	+5.0V

2.12.5 Serial Communications Port #1 Expansion Connector

The Serial Communications Port #1 is an MPIO port attached to the SCI #0 expansion connector. This port can be configured as a Serial Communications Interface or as SPI0 signals. Refer to **Table 2-18** for connection information.

Table 2-18. SCI #1 Connector Description

J17			
Pin #	**Signal**	**Pin #**	**Signal**
1	TXD1 / $\overline{SS0}$	2	RXD1 / MISO0
3	GND	4	+3.3V
5	GND	6	+5.0V

2.12.6 Encoder #0 / Quad Timer Channel A Expansion Connector

The Encoder #0 / Quad Timer Channel A port is an MPIO port attached to the Timer A expansion connector. This port can be configured as a Quadrature Decoder interface port, as a Quad Timer port, or as GPIO. Refer to **Table 2-19** for the signals attached to the connector.

Table 2-19. Timer A Signal Connector Description

J7			
Pin #	**Signal**	**Pin #**	**Signal**
1	PHASEA0 / TA0 / PB7	2	PHASEB0 / TA1 / PB6
3	INDEX0 / TA2 / PB5	4	HOME0 / TA3 / PB4
5	GND	6	+3.3V

2.12.7 Timer Channel C Expansion Connector

The Timer Channel C port is an MPIO port attached to the Timer C expansion connector. This port can be configured as a Quad Timer Interface, as SCI0 signals, or as GPIO. Refer to **Table 2-20** for the signals attached to the connector.

Table 2-20. Timer Channel C Connector Description

J9			
Pin #	**Signal**	**Pin #**	**Signal**
1	TC0 / TXD0 / PC6	2	TC1 / RXD0 / TC5
3	GND	4	TC3 / PC4

2.12.8 FlexCAN Expansion Connector

The FlexCAN port is an MPIO port attached to the FlexCAN expansion connector. This port can be configured as a FlexCAN Interface or as GPIO. Refer to **Table 2-21** for connection information.

Table 2-21. CAN Connector Description

J10			
Pin #	**Signal**	**Pin #**	**Signal**
1	CAN_TX / PC3	2	GND
3	CAN_RX / PC2	4	GND

2.12.9 A/D Port A Expansion Connector

The 8-channel Analog-to-Digital conversion port A is attached to this connector. Refer to **Table 2-22** for connection information. There is an RC network on each of the Analog Port A input signals; see **Figure 2-12**.

Table 2-22. A/D Port A Connector Description

J6			
Pin #	**Signal**	**Pin #**	**Signal**
1	AN0	2	AN1
3	AN2	4	AN3
5	AN4	6	AN5
7	AN6	8	AN7
9	GNDA	10	$+V_{REFH}$

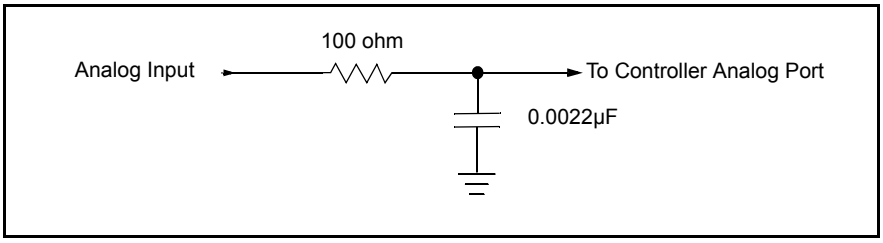

Figure 2-12. Typical Analog Input RC Filter

2.12.10 GPIO Port A Expansion Connector

The GPIO port A is attached to this connector. Refer to **Table 2-23** for connection information.

Table 2-23. GPIO Port A Connector Description

J16			
Pin #	**Signal**	**Pin #**	**Signal**
1	PA0 / PWMA0	2	PA1 / PWMA1
3	PA2 / PWMA2 / $\overline{SS1}$	4	PA3 / MISO1 / PWMA3
5	PA4 / PWMA4 / MOSI1	6	PA5 / SCLK1 / PWMA5
7	PA6 / FAULTA0	8	PA7 / FAULTA1
9	PA8 / FAULTA2	10	PA9 / ISA0
11	PA10 / ISA1	12	PA11 / ISA2
13	GND	14	+3.3V

2.12.11 GPIO Port B Expansion Connector

The GPIO port B is attached to this connector. Refer to **Table 2-24** for connection information.

Table 2-24. GPIO Port B Connector Description

J18			
Pin #	**Signal**	**Pin #**	**Signal**
1	PB0 / $\overline{SS0}$	2	PB1 / MISO0
3	PB2 / MOSI0	4	PB3 / SCLK0
5	PB4 / HOME0	6	PB5 / INDEX0
7	PB6 / PHASEB0	8	PB7 / PHASEA0
9	GND	10	+3.3V

2.12.12 GPIO Port C Expansion Connector

The GPIO port C is attached to this connector. Refer to **Table 2-25** for connection information.

Table 2-25. GPIO Port C Connector Description

J19			
Pin #	**Signal**	**Pin #**	**Signal**
1	PC0 / EXTAL	2	PC1 / XTAL
3	PC2 / CAN_RX	4	PC3 / CAN_TX
5	PC4 / TC3	6	PC5 / TC1
7	PC6 / TC0	8	NC
9	GND	10	+3.3V

2.12.13 IRQA / RESET / CLOCK Expansion Connector

The IRQA / RESET / CLOCK signals are attached to this connector. Refer to **Table 2-26** for connection information.

Table 2-26. IRQA / RESET / CLOCK Connector Description

J11			
Pin #	**Signal**	**Pin #**	**Signal**
1	$\overline{\text{IRQA}}$	2	$\overline{\text{RESET}}$
3	EXTAL / PC0	4	XTAL / PC1
9	GND	10	+3.3V

2.13 Test Points

The 56F8323EVM board has a total of eleven test points:

- Analog Ground (AGND) [TP4]
- Four Digital Grounds (GND) [TP1, TP2, TP3 & TP10]
- Two +3.3V [TP6 & TP11]
- +3.3VA [TP5]
- Two +5.0V [TP7 & TP8]
- +12V [TP9]

Appendix A
56F8323EVM Schematics

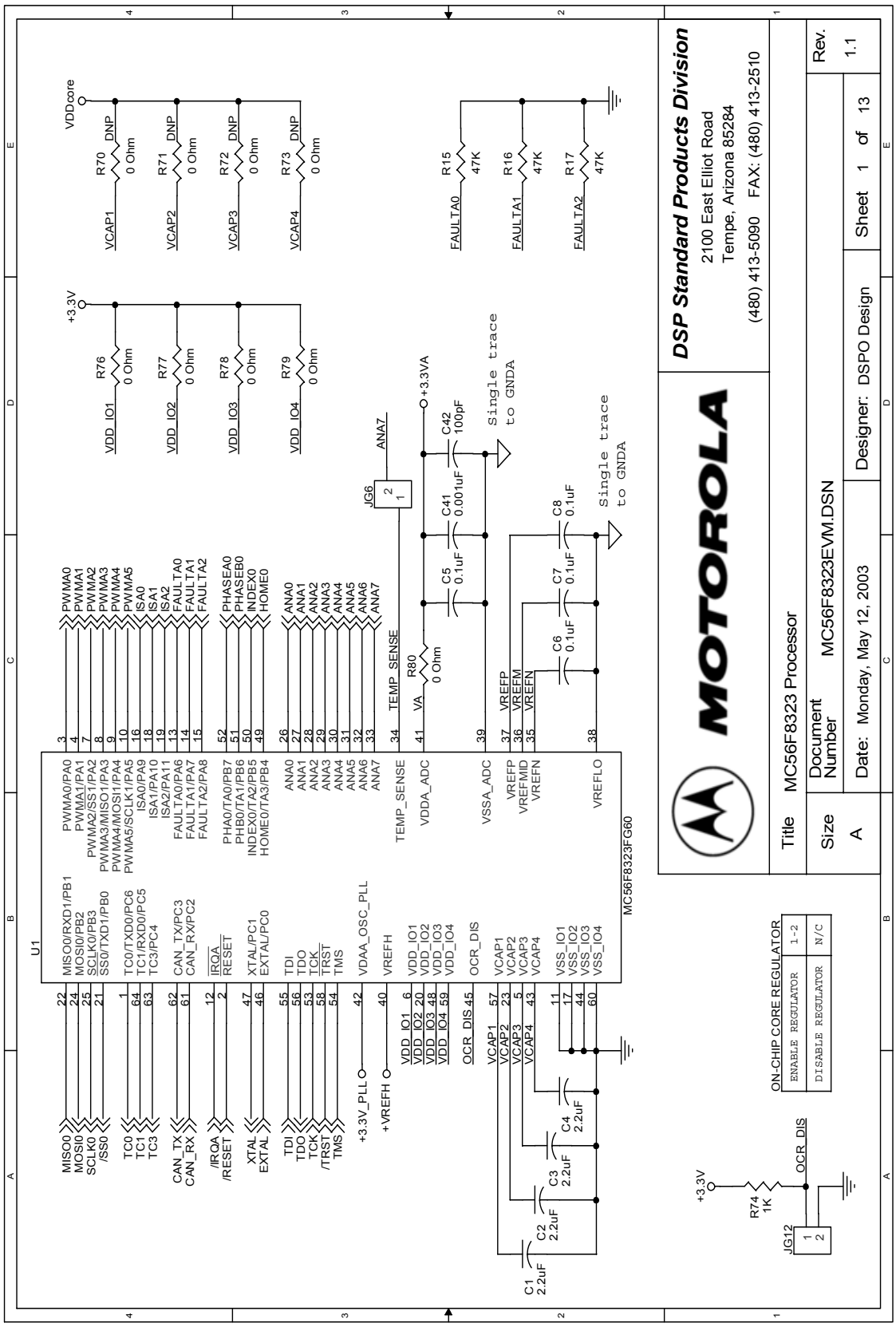

Figure A-1. 56F8323 Processor

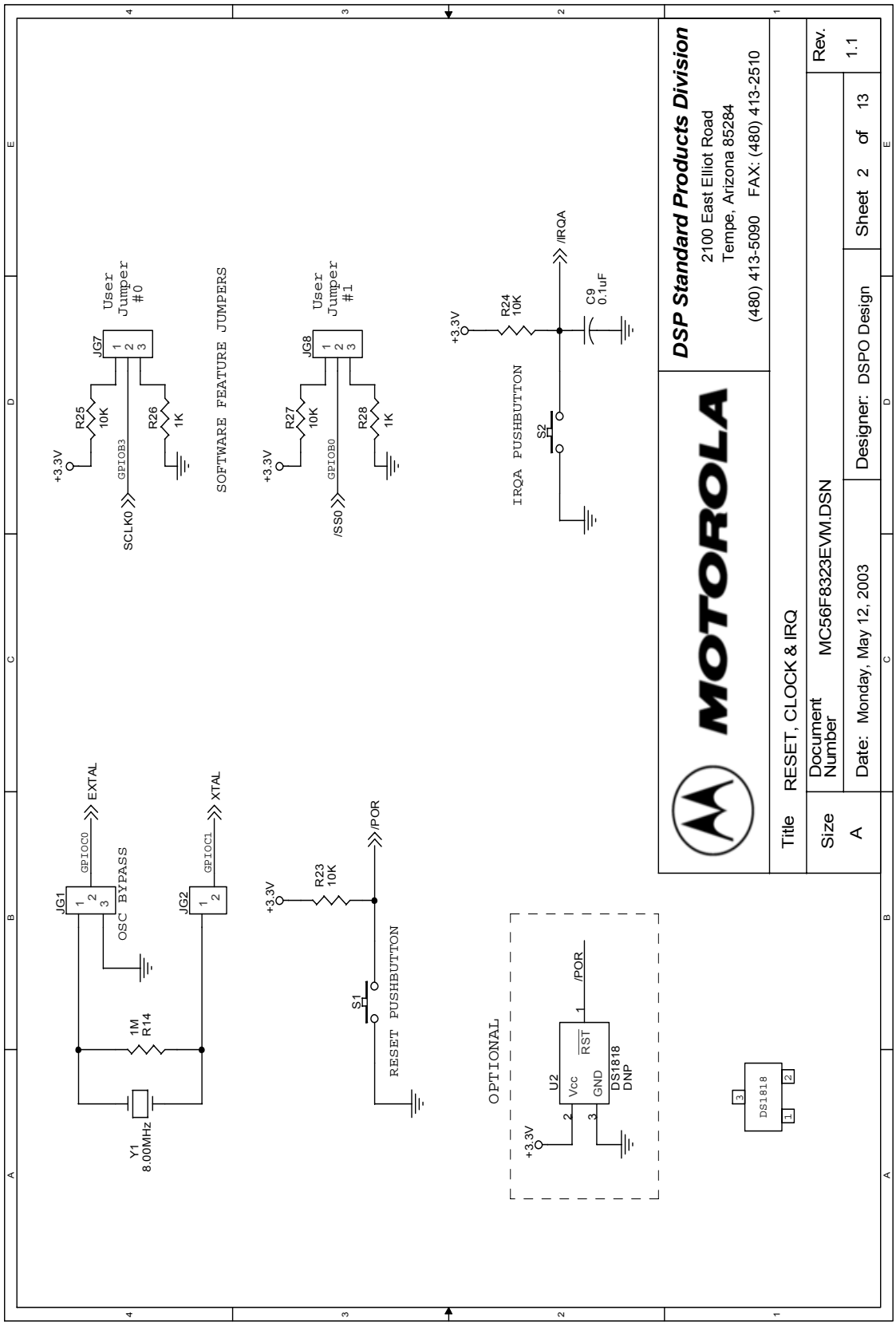

Figure A-2. Reset, Clock & IRQ

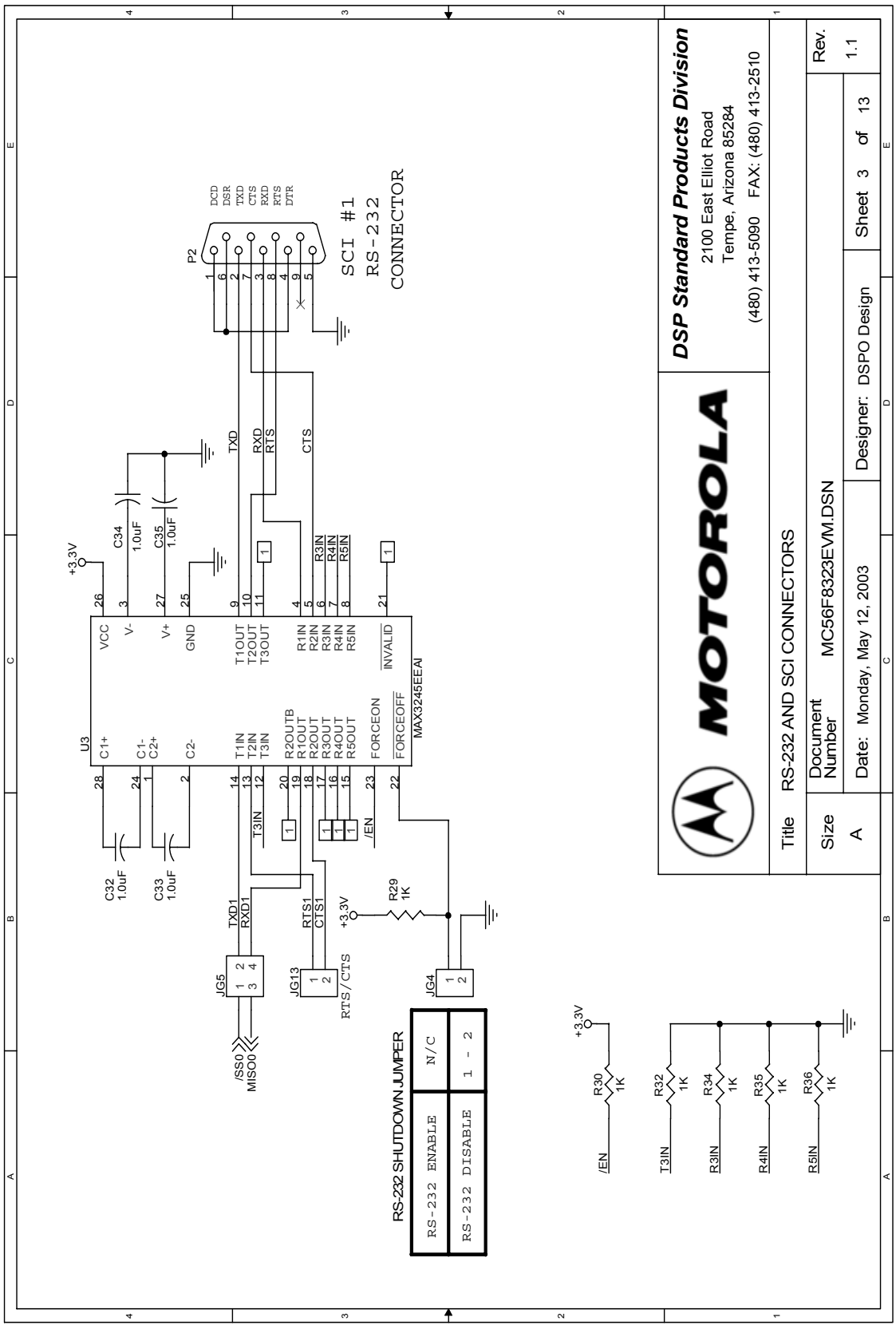

Figure A-3. RS-232 and SCI Connectors

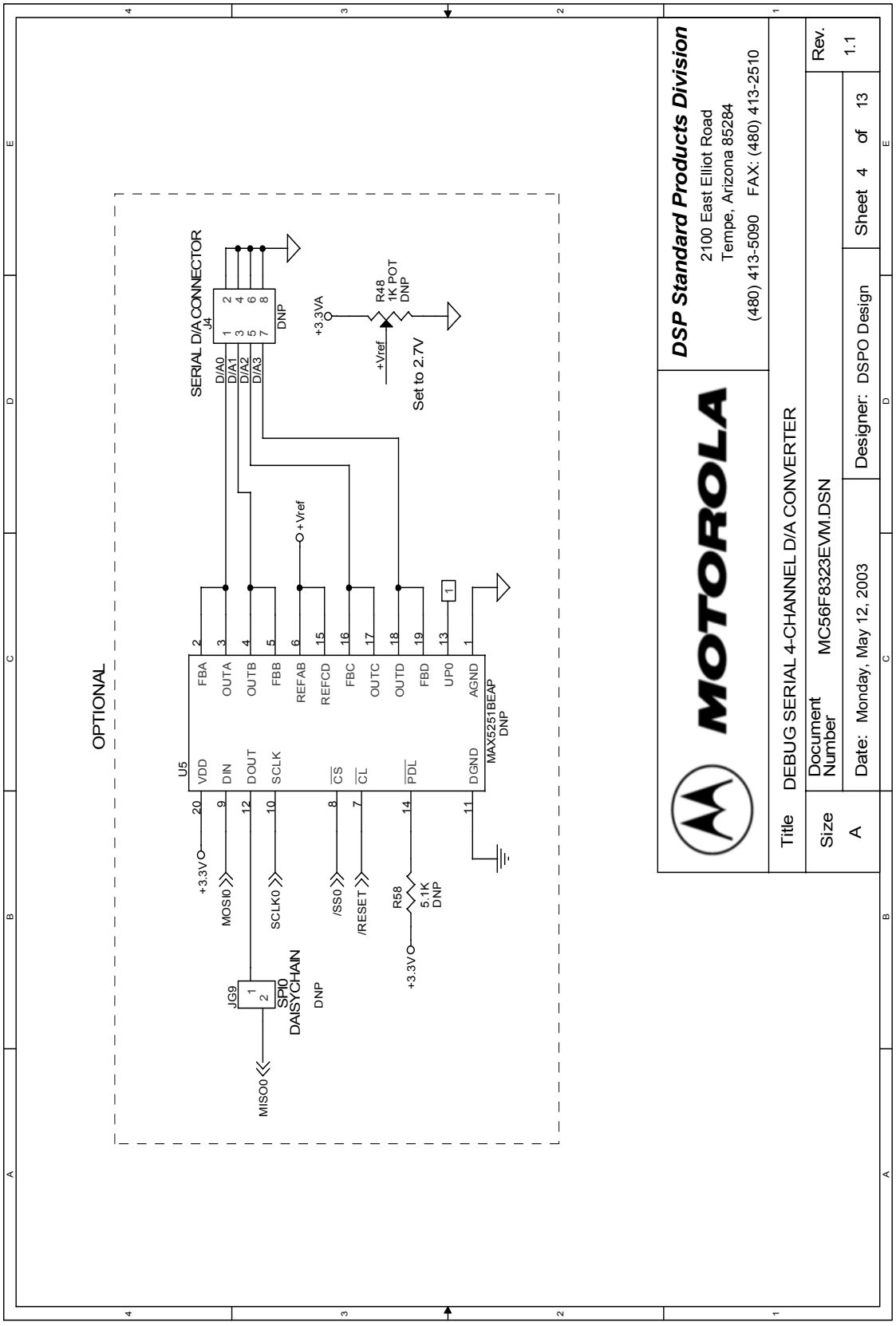

Figure A-4. Debug Serial 4-Channel D/A Converter

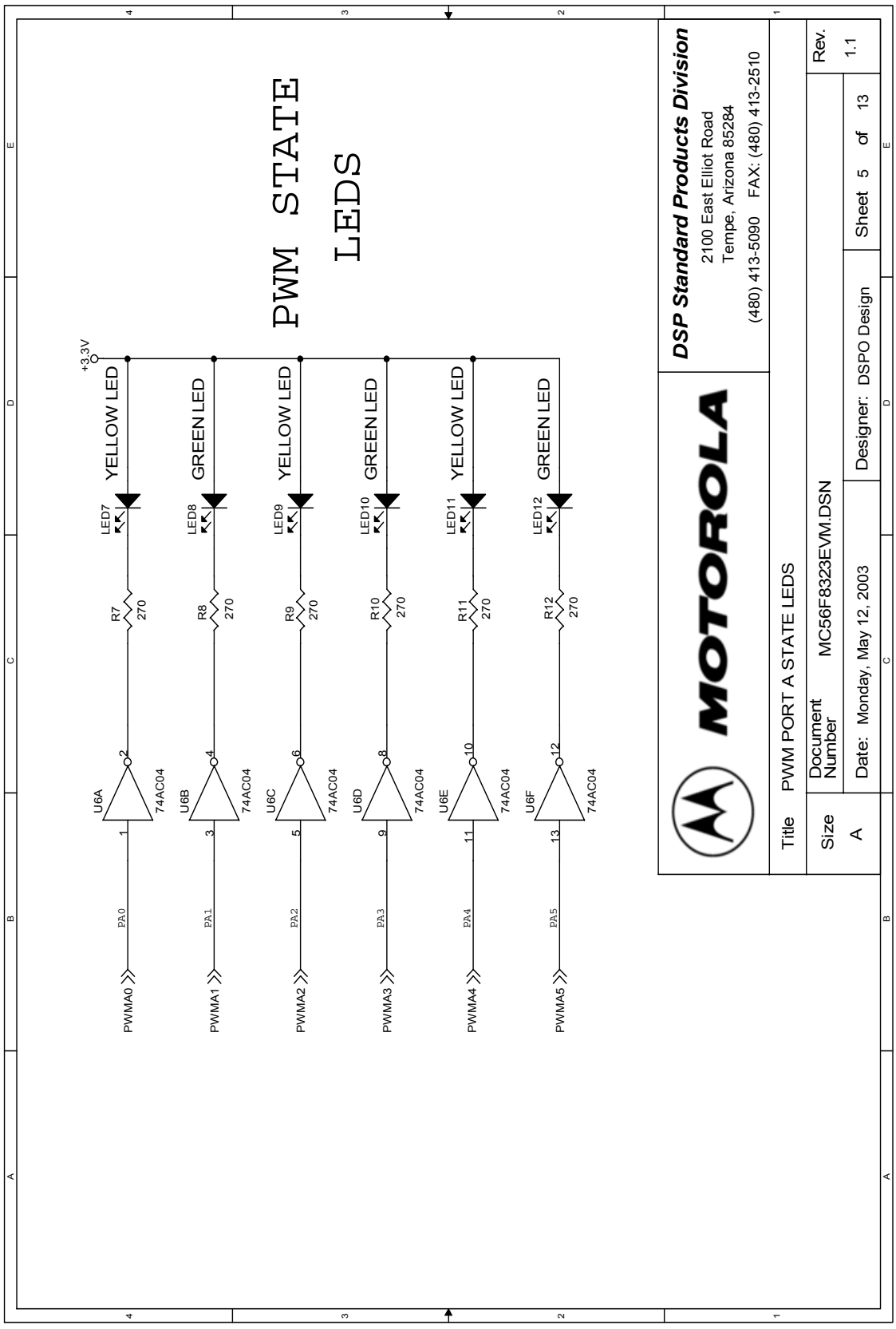

Figure A-5. PWM Port A State LEDs

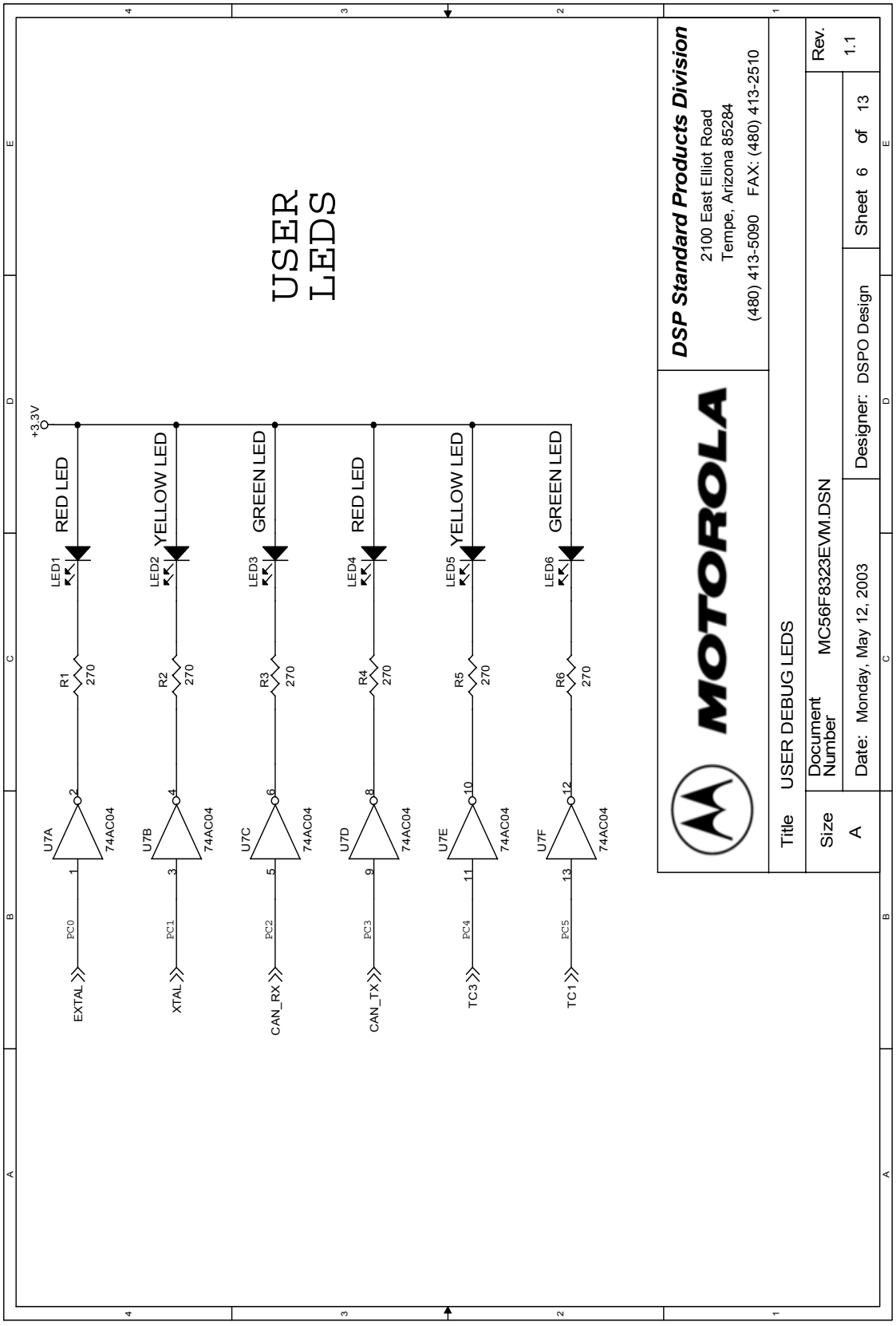

Figure A-6. User Debug LEDs

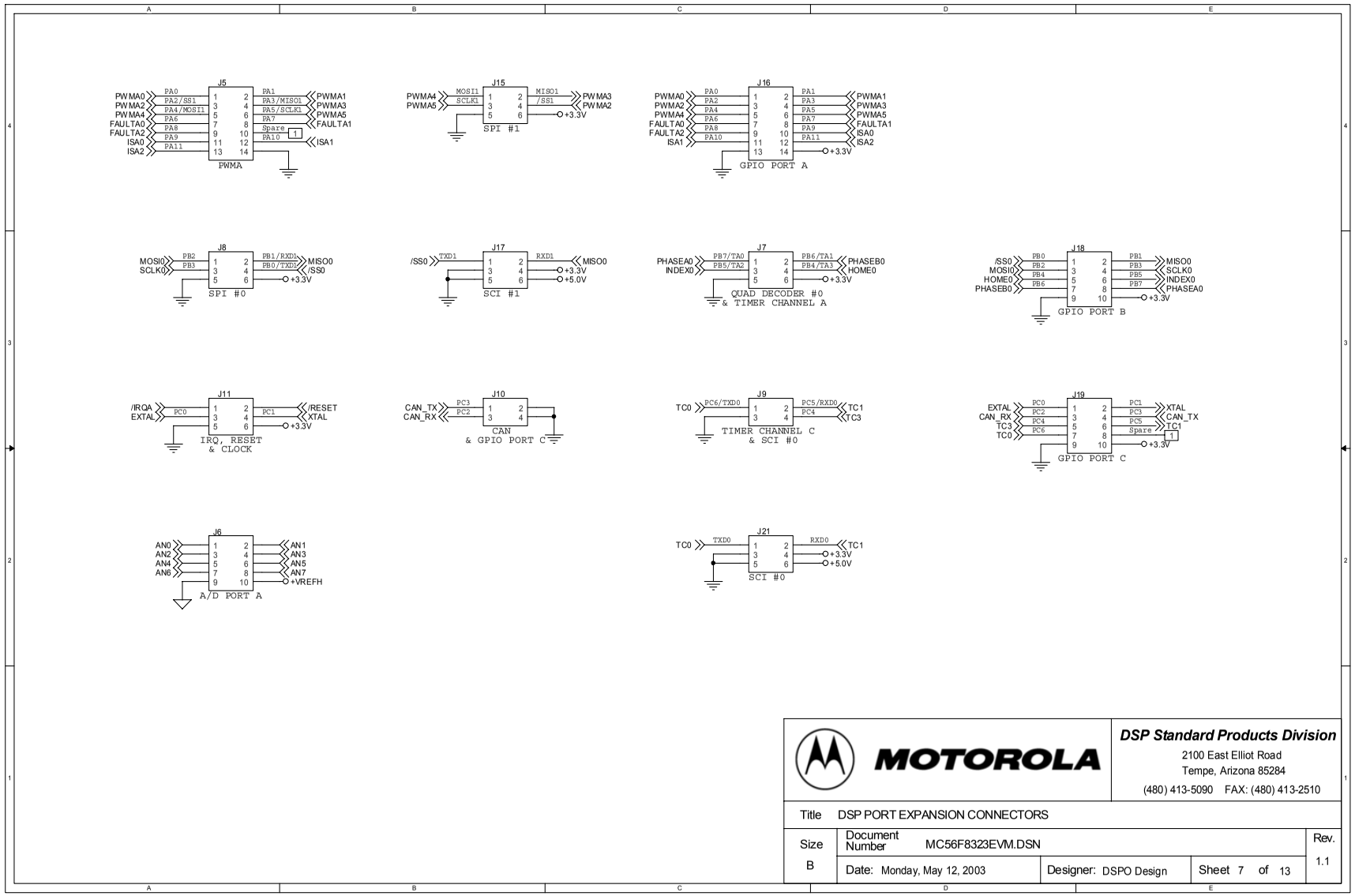

Figure A-7. Port Expansion Connectors

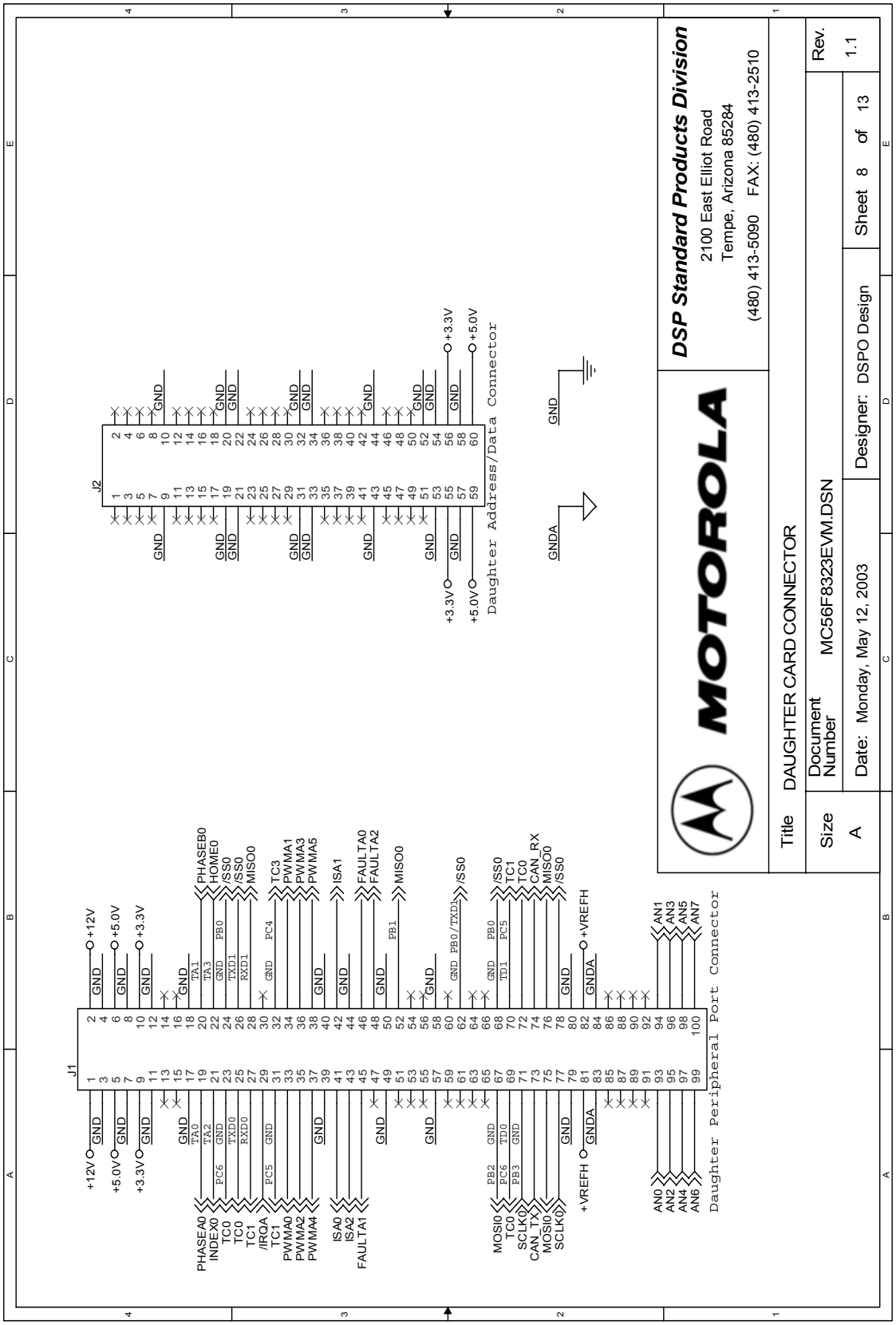

Figure A-8. Daughter Card Connectors

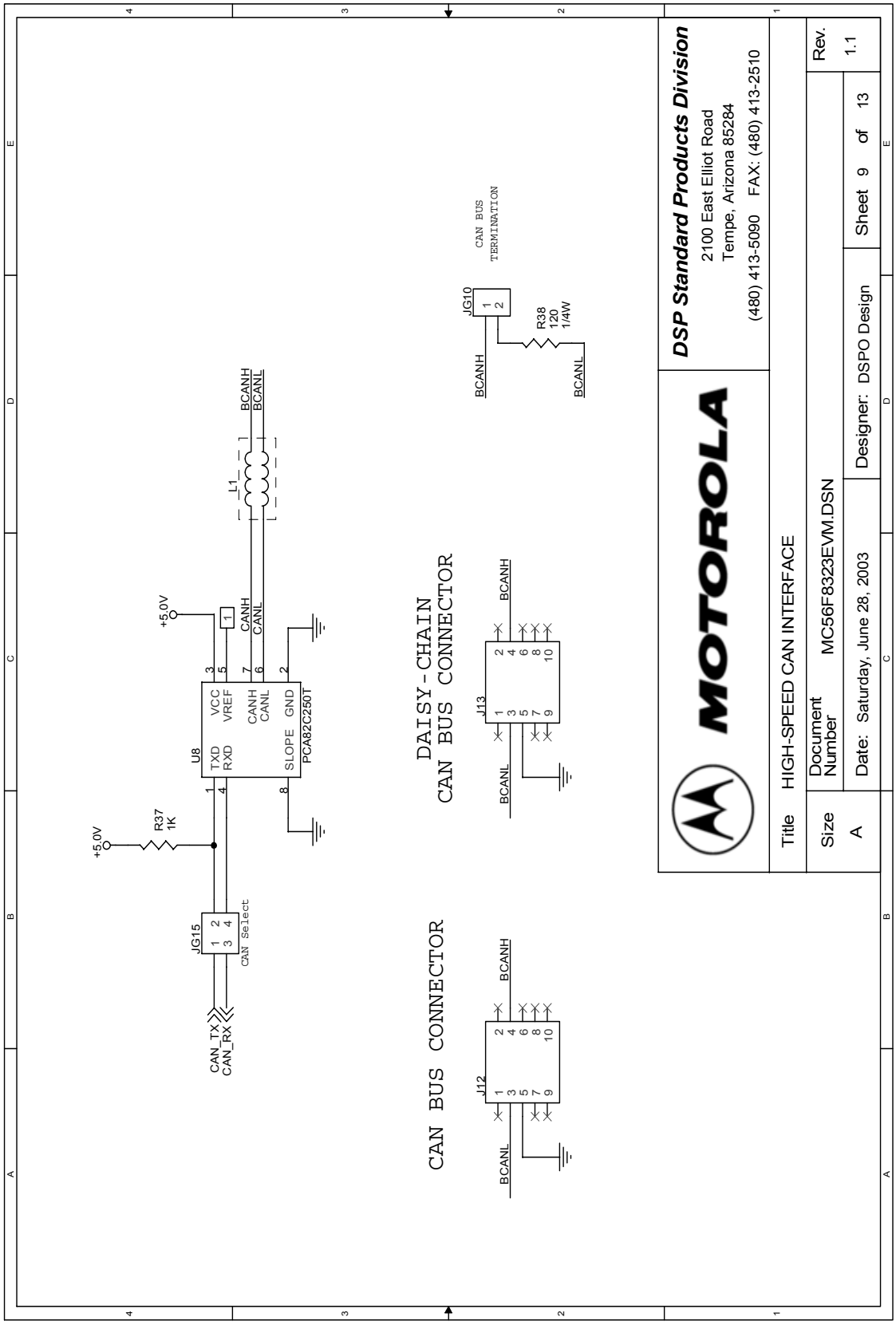

Figure A-9. High-Speed CAN Interface

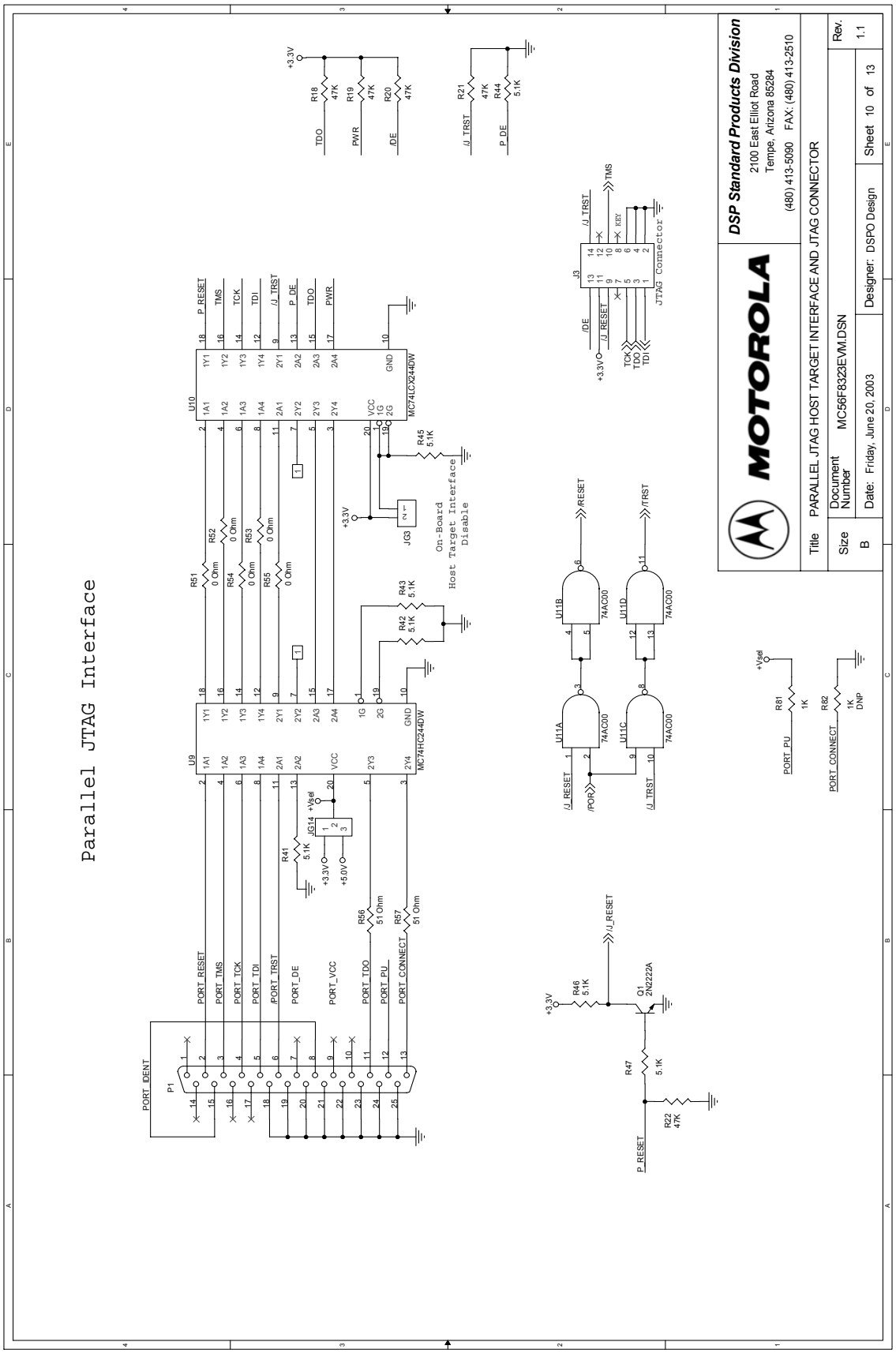

Figure A-10. Parallel JTAG Host Target Interface and JTAG Connector

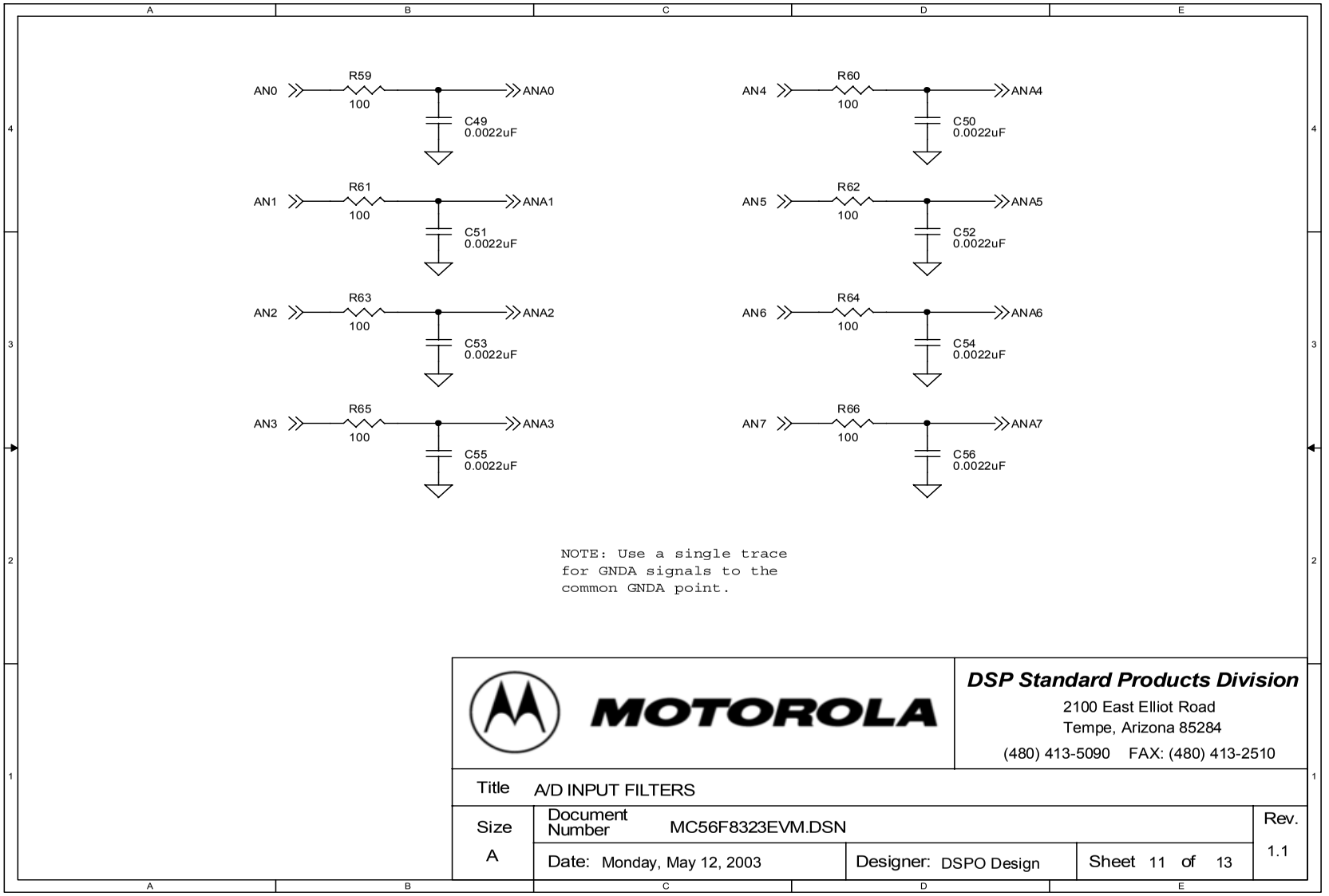

Figure A-11. A/D Input Filters

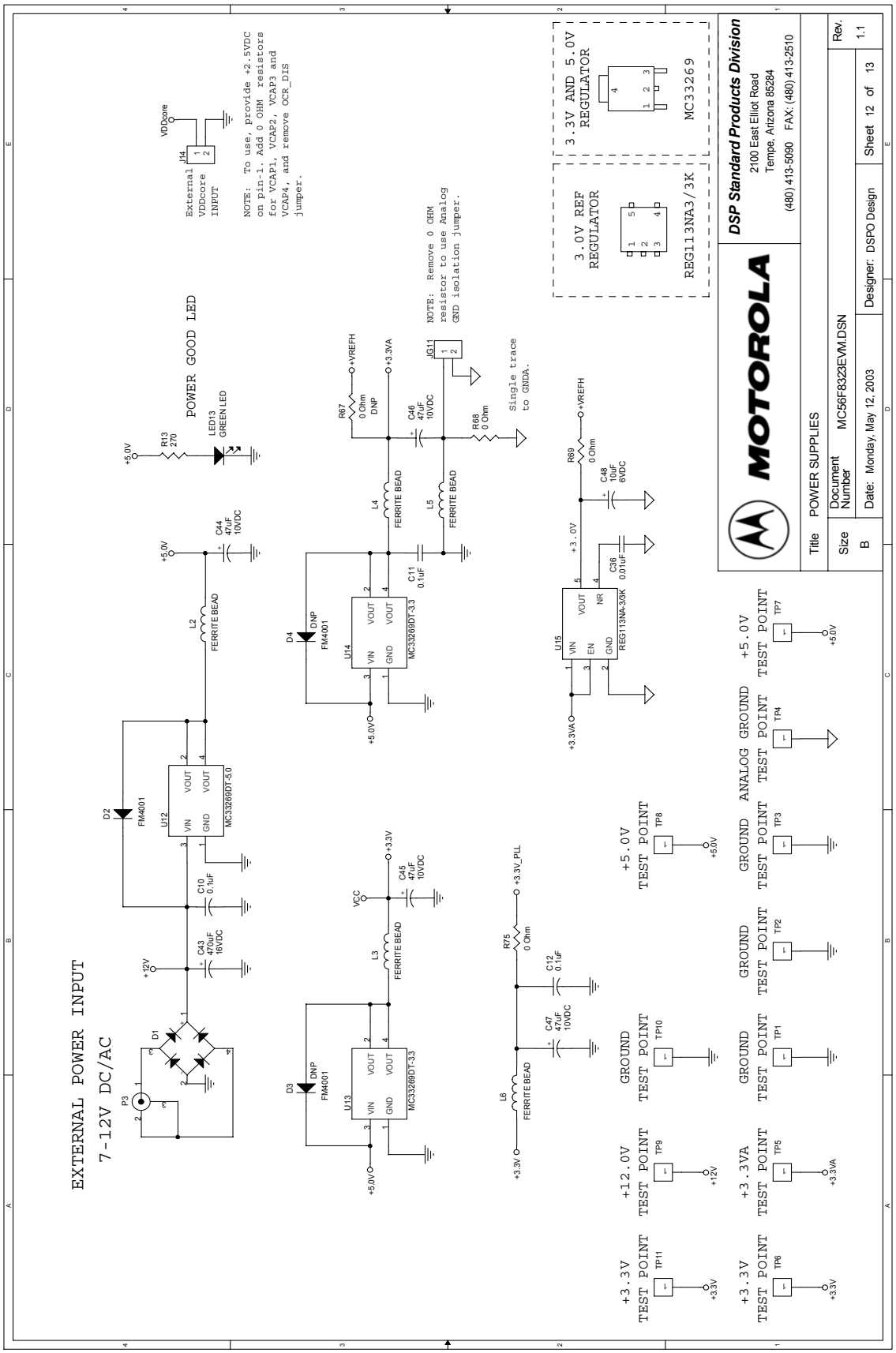

Figure A-12. Power Supplies

56F8323EVM Schematics, Rev. 2

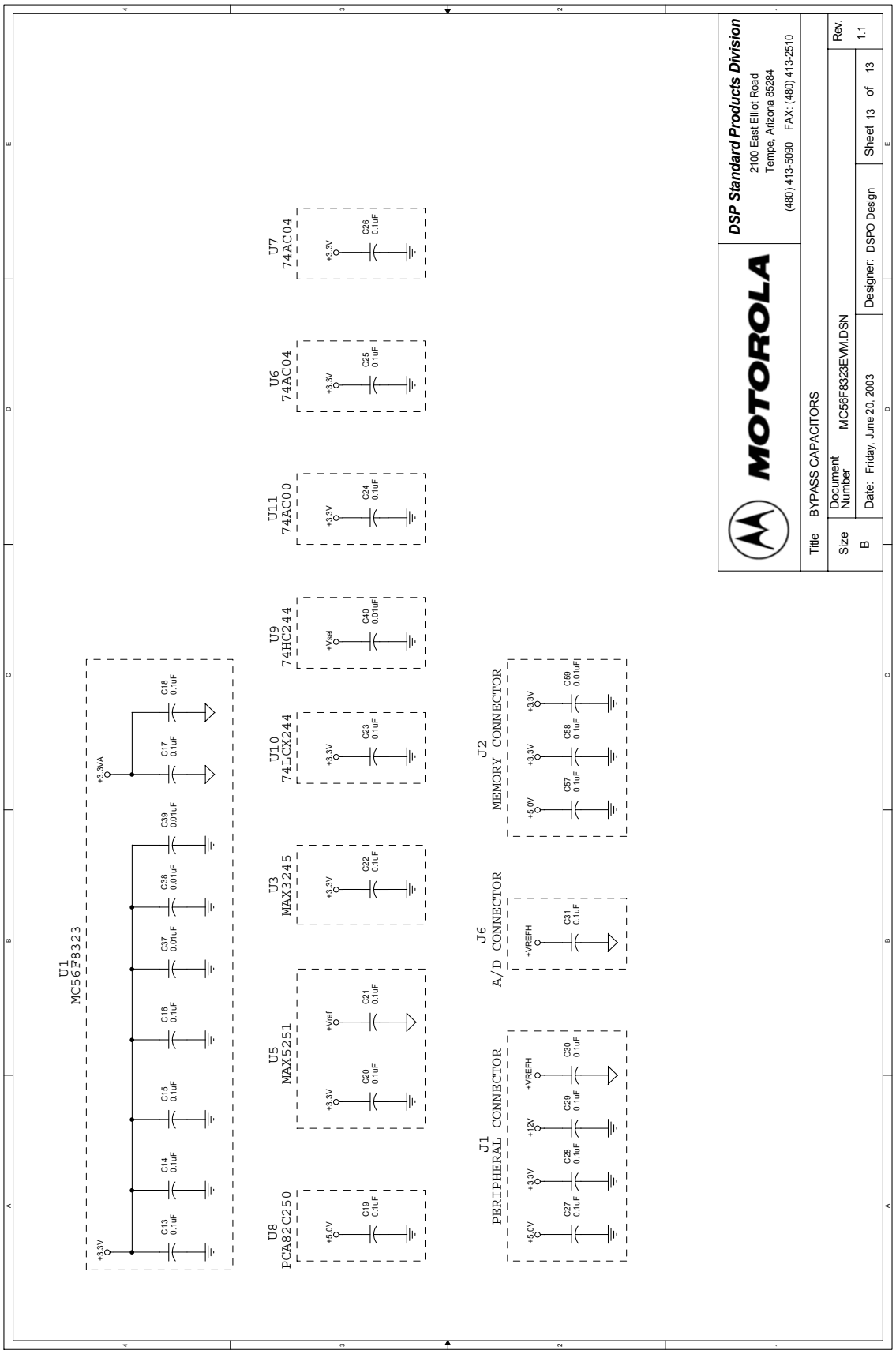

Figure A-13. Bypass Capacitors

Appendix B
56F8323EVM Bill of Material

Qty	Description	Ref. Designators	Vendor Part #
Integrated Circuits			
1	MC56F8323	U1	Freescale Semiconductor, MC56F8323VFB60
0	Power-On Reset	U2 (Optional)	Dallas Semiconductor, DS1818
1	RS-232 Transceiver	U3	Maxim, MAX3245EEAI
0	SPI 4-Channel D/A	U5 (Optional)	Maxim, MAX5251BEAP
2	74AC04	U6, U7	ON Semiconductor, MC74AC04AD
1	CAN Transceiver	U8	Philips Semiconductor, PCA82C250T
1	74HC244	U9	ON Semiconductor, MC74LHC44AADW
1	74LCX244	U10	ON Semiconductor, MC74LCX244ADW
1	74AC00	U11	Fairchild, 74AC00SC
1	+5.0V Voltage Regulator	U12	ON Semiconductor, MC33269DT-5
2	+3.3V Voltage Regulator	U13, U14	ON Semiconductor, MC33269DT-3.3
1	+3.0V Voltage Regulator	U15	Burr-Brown, REG113NA-3/3K
Resistors			
13	270 Ω	R1–R13	SMEC, RC73L2A271OHMJT
1	1M Ω	R14	SMEC, RC73L2A105OHMJT
8	47K Ω	R15–R22	SMEC, RC73L2A473OHMJT
4	10K Ω	R23, R24, R25, R27	SMEC, RC73L2A103OHMJT
11	1K Ω	R26, R28–R30, R32, R34–R37, R74, R81	SMEC, RC73L2A103OHMJT

Qty	Description	Ref. Designators	Vendor Part #
Resistors (Continued)			
1	120 Ω, 1/4W	R38	YAGEO, CFR 120QBK
7	5.1K Ω	R41–R47	SMEC, RC73L2A512OHMJT
13	0 Ω	R51–R55, R68, R69, R75–R80	SMEC, RC73JP2A
2	51 Ω	R56, R57	SMEC, RC73L2A51OHMJT
0	5.1K Ω	R58 (Optional)	SMEC, RC73L2A512OHMJT
8	100 Ω	R59–R66	SMEC, RC73L2A101OHMJT
0	0 Ω	R67, R70–R73 (Optional)	SMEC, RC73JP2A
0	1K Ω	R82 (Optional)	SMEC, RC73L2A103OHMJT
Potentioneters			
0	1K Ω	R48 (Optional)	BC/MEPCOPAL, ST4B102CT
Inductors			
1	CAN Bus Filter	L1	EPCOS, B82790-S0513-N201
5	1.0mH FERRITE BEAD	L2–L6	Panasonic, EXC-ELSA35V
LEDs			
2	Red LED	LED1, LED4	Hewlett-Packard, HSMS-C650
5	Yellow LED	LED2, LED5, LED7, LED9, LED11	Hewlett-Packard, HSMY-C650
6	Green LED	LED3, LED6, LED8, LED10, LED12, LED13	Hewlett-Packard, HSMG-C650
Diode			
1	+50V 1A BRIDGE RECT	D1	DIODES, DF02S
1	S2B-FM401	D2	Vishay, DL4001DICT
0	S2B-FM401	D3 & D4 (Optional)	Vishay, DL4001DICT
Capacitors			
4	2.2μF, +25V DC (Low ESR)	C1–C4	TAIYO YUDEN, CELMK212BJ225MG-T
29	0.1μF	C5–C31, C57, C58	SMEC, MCCE104K2NR-T1
4	1.0μF, +25V DC	C32–C35	SMEC, MCCE105K3NR-T1

Qty	Description	Ref. Designators	Vendor Part #
Capacitors (Continued)			
6	0.01μF	C36–C40, C59	SMEC, MCCE103K2NR-T1
1	0.001μF	C41	SMEC, MCCE102K2NR-T1
1	100pF	C42	SMEC, MCCE101K2NR-T1
1	470μF, +16V DC	C43	ELMA, RV-16V471MH10R
4	47μF, +16V DC	C44–C47	ELMA, RV2-16V470M-R
1	10μF, +10V DC	C48	KEMET, T494B106M010AS
8	0.0022μF	C49–C56	SMEC, MCCE222K2NR-T1
Jumpers			
4	3 × 1 Bergstick	JG1, JG7, JG8, JG14	SAMTEC, TSW-103-07-S-S
8	1 × 2 Bergstick	JG2, JG3, JG4, JG6, JG10, JG11, JG12, JG13	SAMTEC, TSW-102-07-S-S
2	2 × 2 Bergstick	JG5, JG15	SAMTEC, TSW-102-07-S-D
0	1 × 2 Bergstick	JG9 (Optional)	SAMTEC, TSW-102-07-S-S
Test Points			
4	GND Test Point	TP1–TP3, TP10	KEYSTONE, 5001 (BLACK)
1	GNDA Test Point	TP4	KEYSTONE, 5002 (WHITE)
1	+3.3VA Test Point	TP5	KEYSTONE, 5004 (YELLOW)
2	+3.3V Test Point	TP6, TP11	KEYSTONE, 5000 (RED)
1	+5.0V & +12V Test Point	TP7, TP8, TP9	KEYSTONE, 5003 (ORANGE)
0	1 × 1 Bergstick	T15, T16 (Optional)	Samtec, TSW-101-06-S-S
Crystals			
1	8.00MHz Crystal	Y1	CTS, ATS08ASM-T
Connectors			
1	DB25M Connector	P1	AMPHENOL, 617-C025P-AJ121
1	DE9S Connector	P2	AMPHENOL, 617-C009S-AJ120
1	2.1mm coax Power Connector	P3	Switchcraft, RAPC-722

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Qty	Description	Ref. Designators	Vendor Part #
Connectors (Continued)			
1	Peripheral Daughter Card Connector	J1	HRS, FX6-100P-0.8SV2
1	Memory Bus Daughter Card Connector	J2	HRS, FX6-60P-0.8SV2
1	7x2 JTAG Header	J3	SAMTEC, TSW-107-07-S-D
0	4x2 Header	J4 (Optional)	SAMTEC, TSW-104-07-S-D
5	5x2 Header	J6, J12, J13, J18, J19	SAMTEC, TSW-105-07-S-D
2	7x2 Header	J5, J16	SAMTEC, TSW-107-07-S-D
5	3x2 Header	J7, J8, J11, J15, J17, J21	SAMTEC, TSW-103-07-S-D
2	2x2 Header	J9, J10	SAMTEC, TSW-102-07-S-D
1	1x2 Header	J14	SAMTEC, TSW-102-07-S-S
Switches			
2	SPST Pushbutton	S1–S2	Panasonic, EVQ-PAD05R
Transistors			
1	2N2222A	Q1	ZETEX, FMMT2222ACT
Miscellaneous			
13	Shunt	SH1–SH13	Samtec, SNT-100-BL-T
4	Rubber Feet	RF1–RF4	3M, SJ5018BLKC

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MC56F8323EVMUM
Rev. 2
07/2005